

20

CENTRAL OFFICE SWITCH

FEEDER 12

SONET

RDT 24

COMMON EQUIPMENT SHELF (CES) 26

CHANNEL BANK SHELF (CHS) 28

HIGH-DENSITY POTS CHANNEL BANK SHELF (HDCB) 30

POTS, ISDN, SPECIALS, T1, FITL

POTS, LIMITED SPECIALS

EXTENSIONS: T1, T3, STS-1, OC-3

FIG. 1

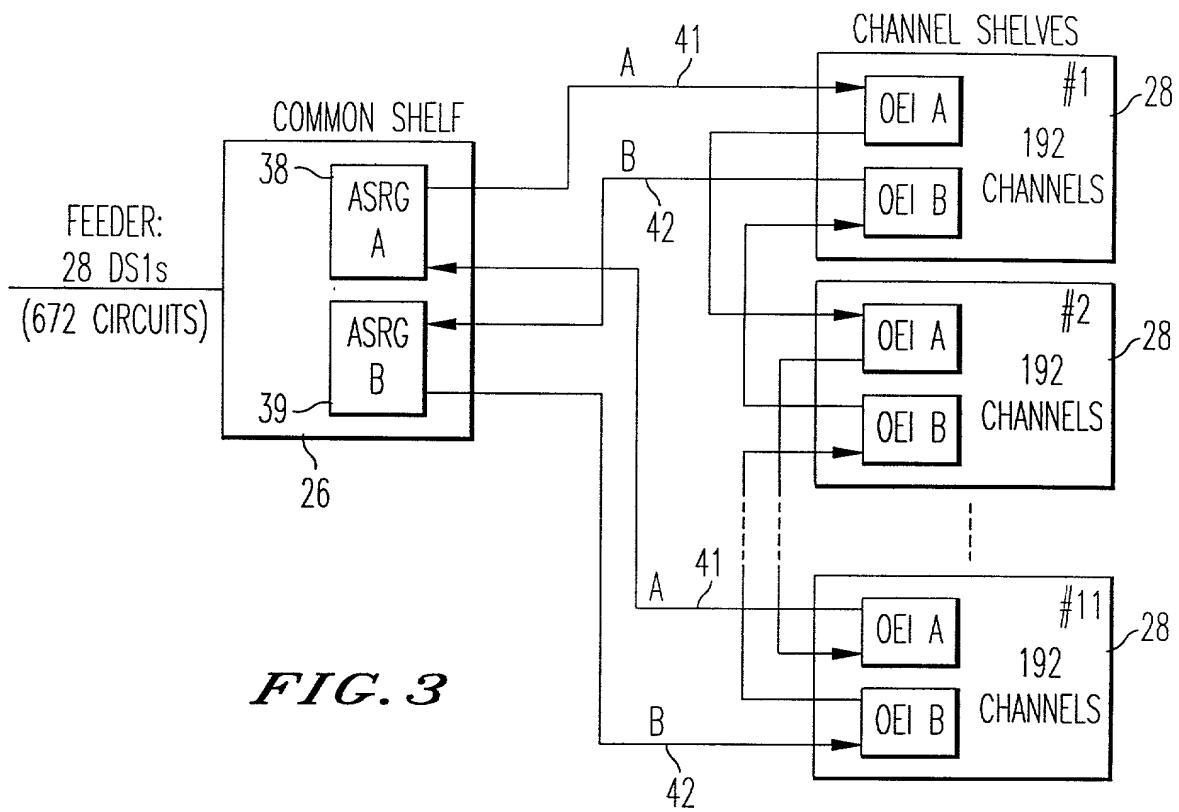


FIG. 3

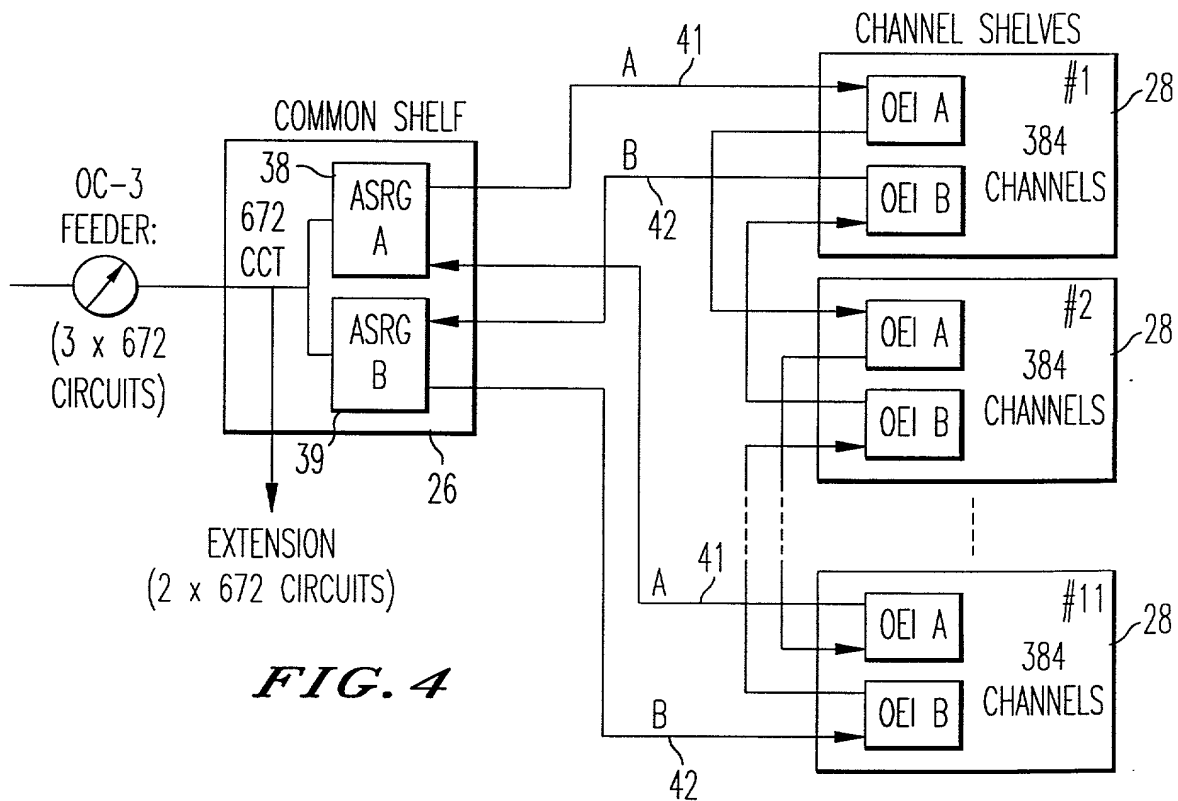
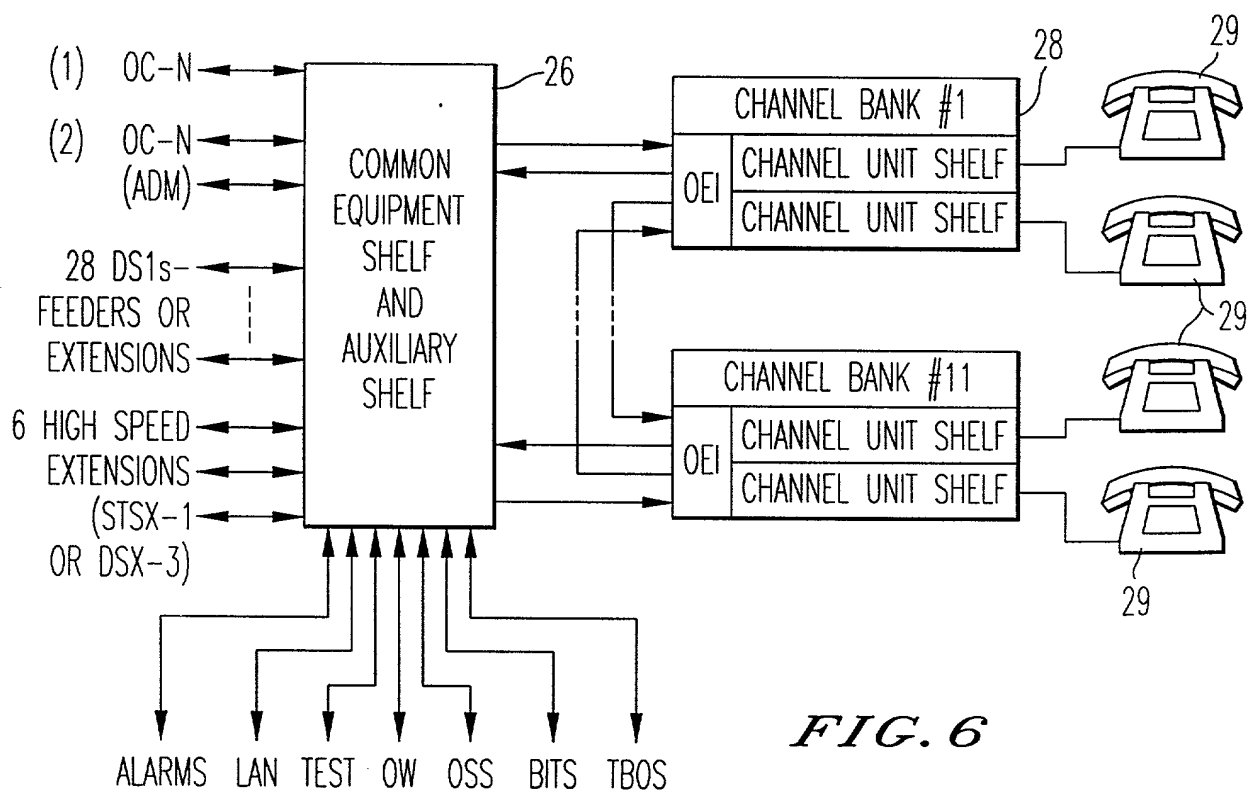
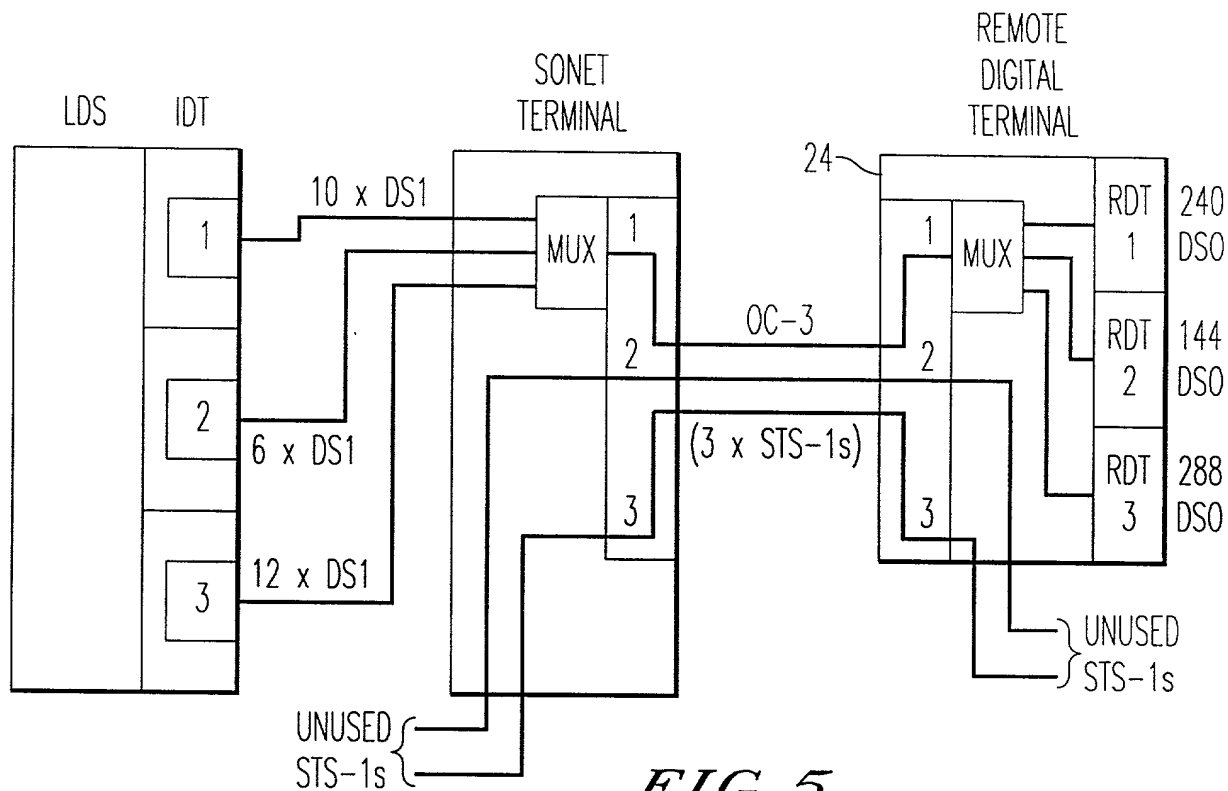


FIG. 4



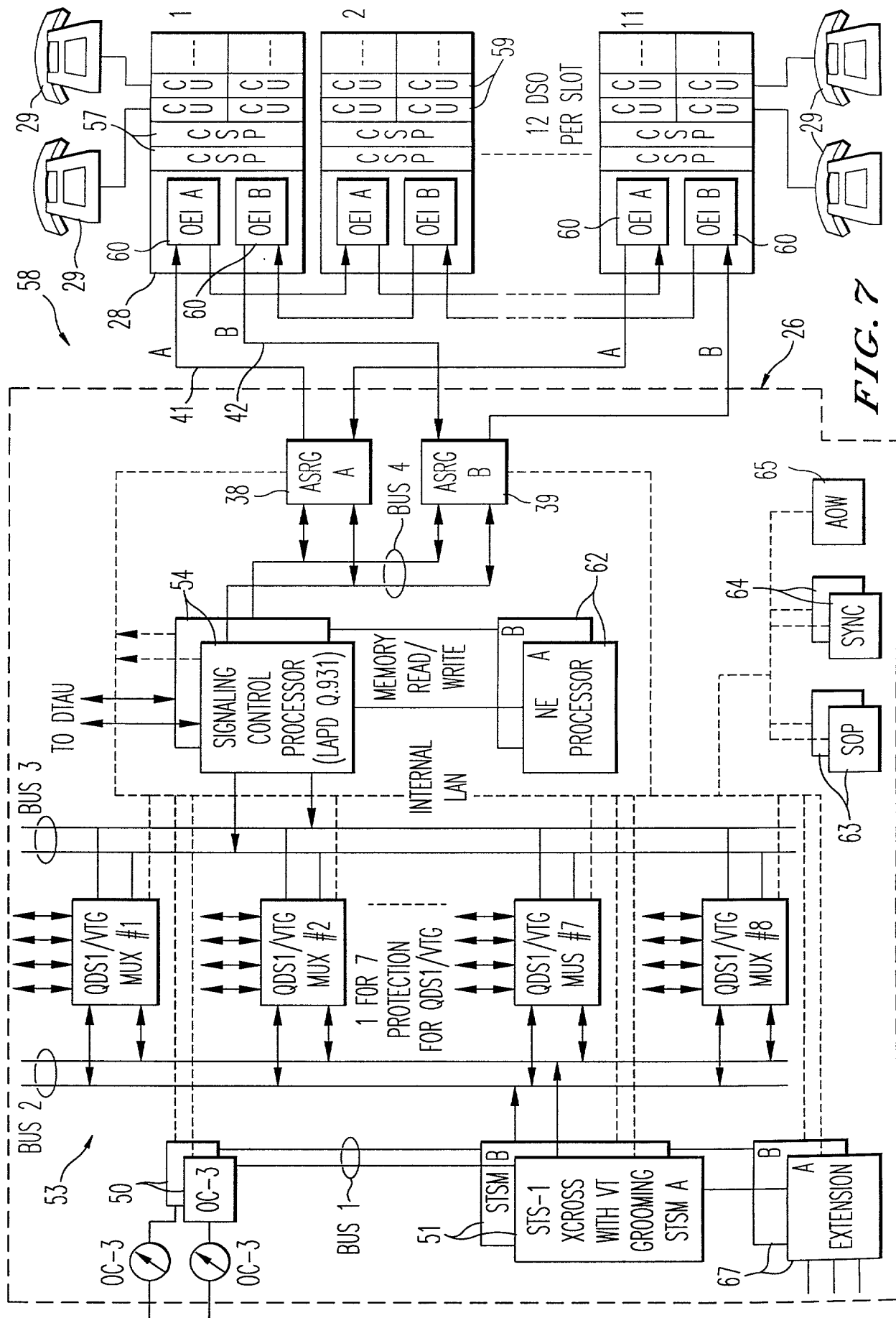


FIG. 7

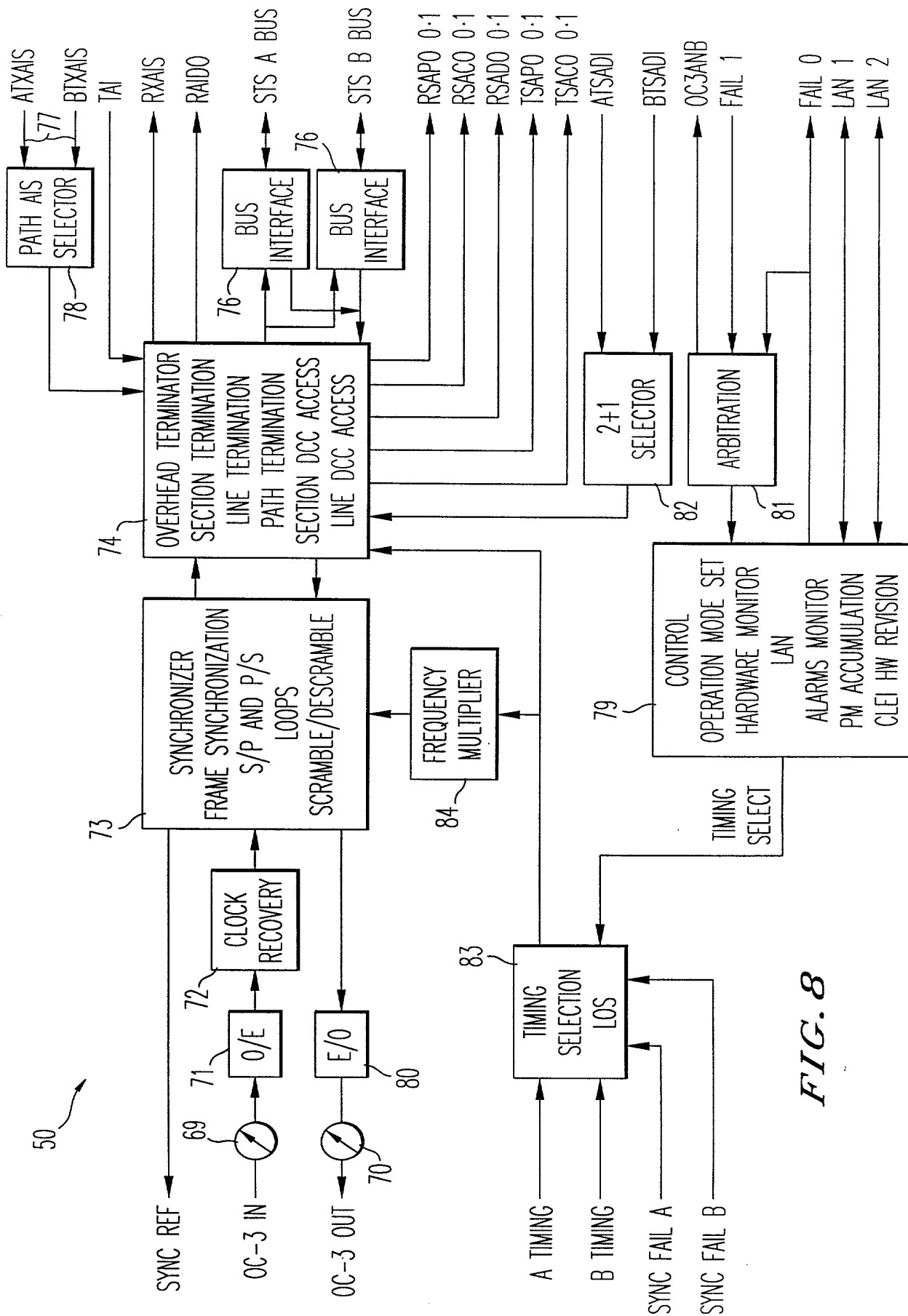


FIG. 8

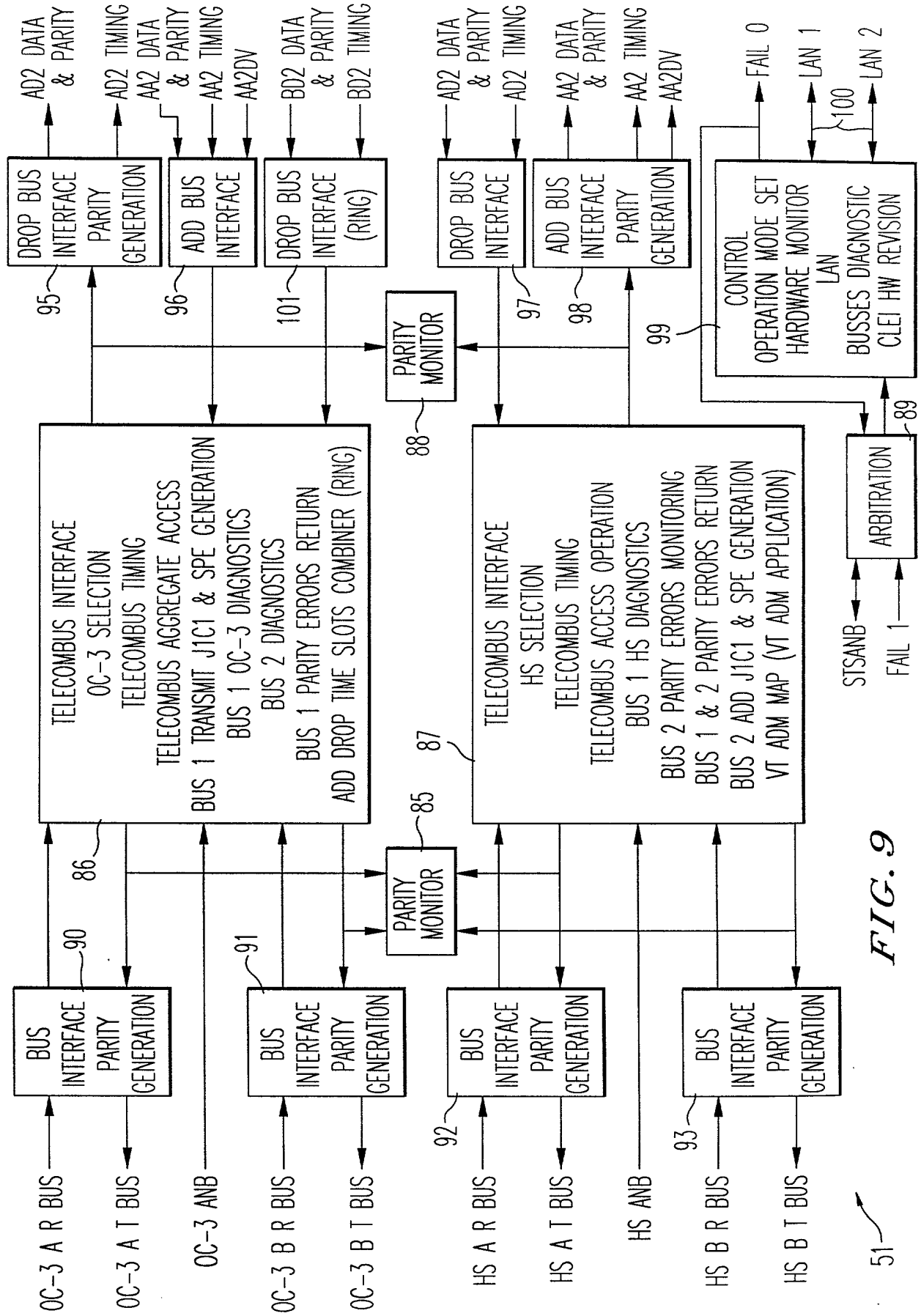


FIG. 9

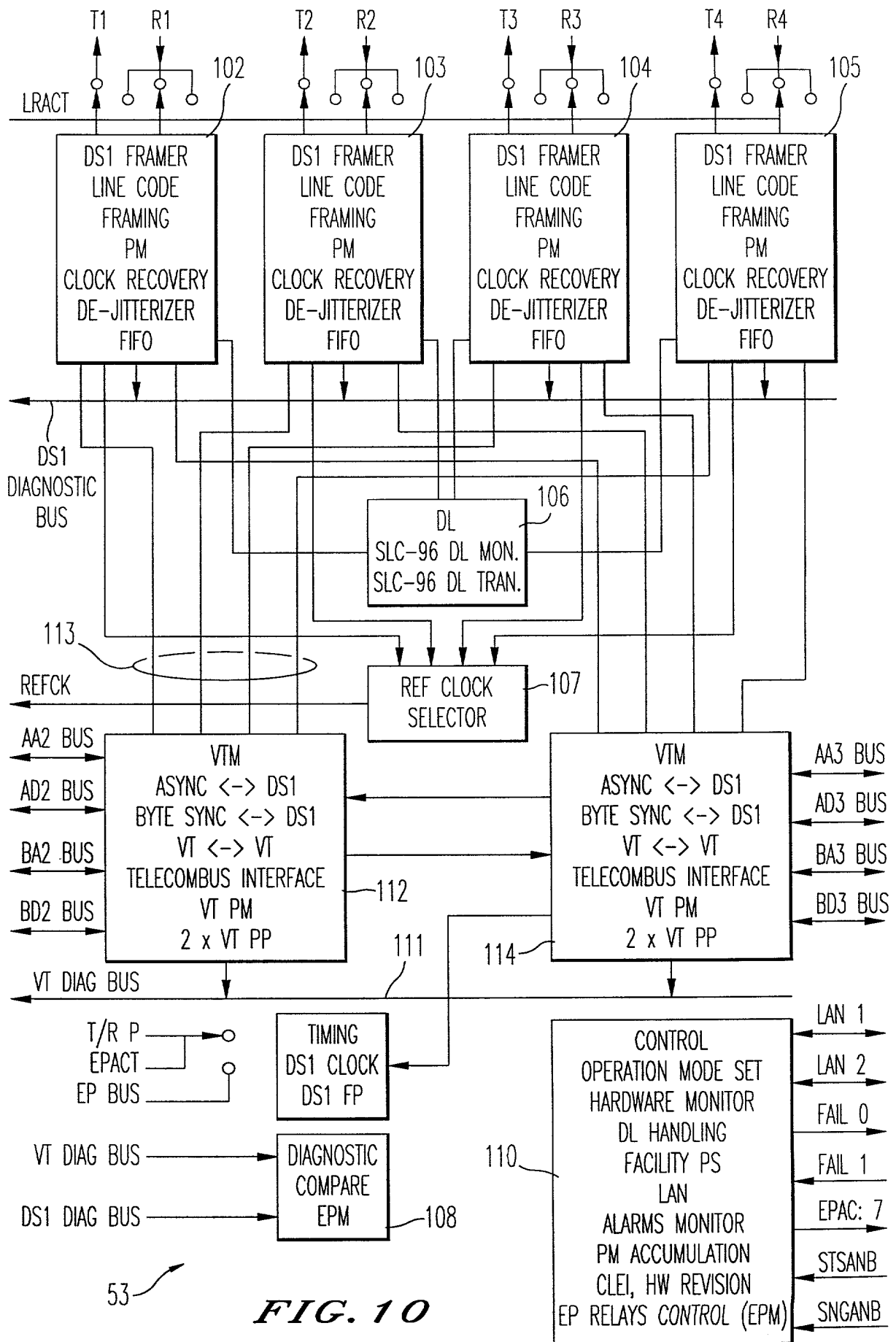


FIG. 10

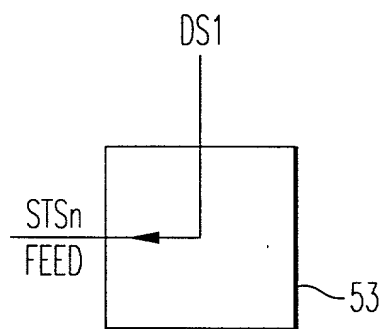


FIG. 11A

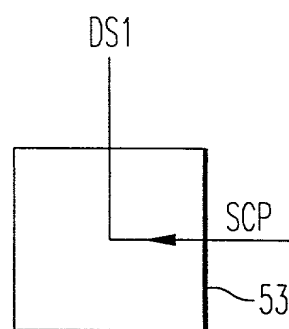


FIG. 11D

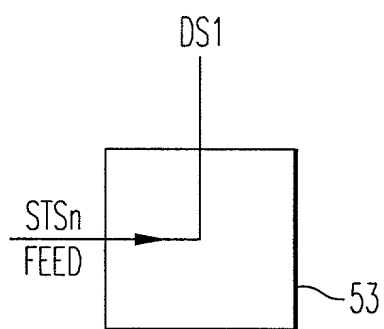


FIG. 11B

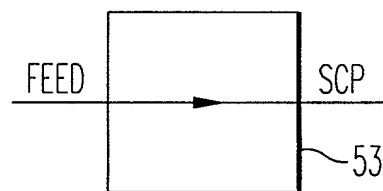


FIG. 11E

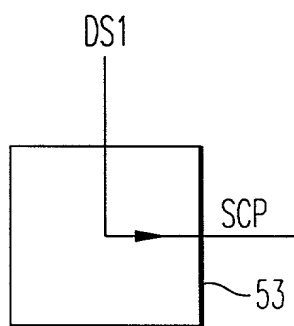


FIG. 11C

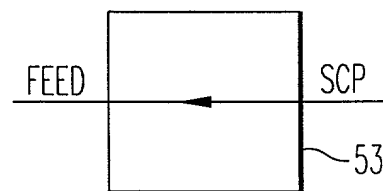


FIG. 11F

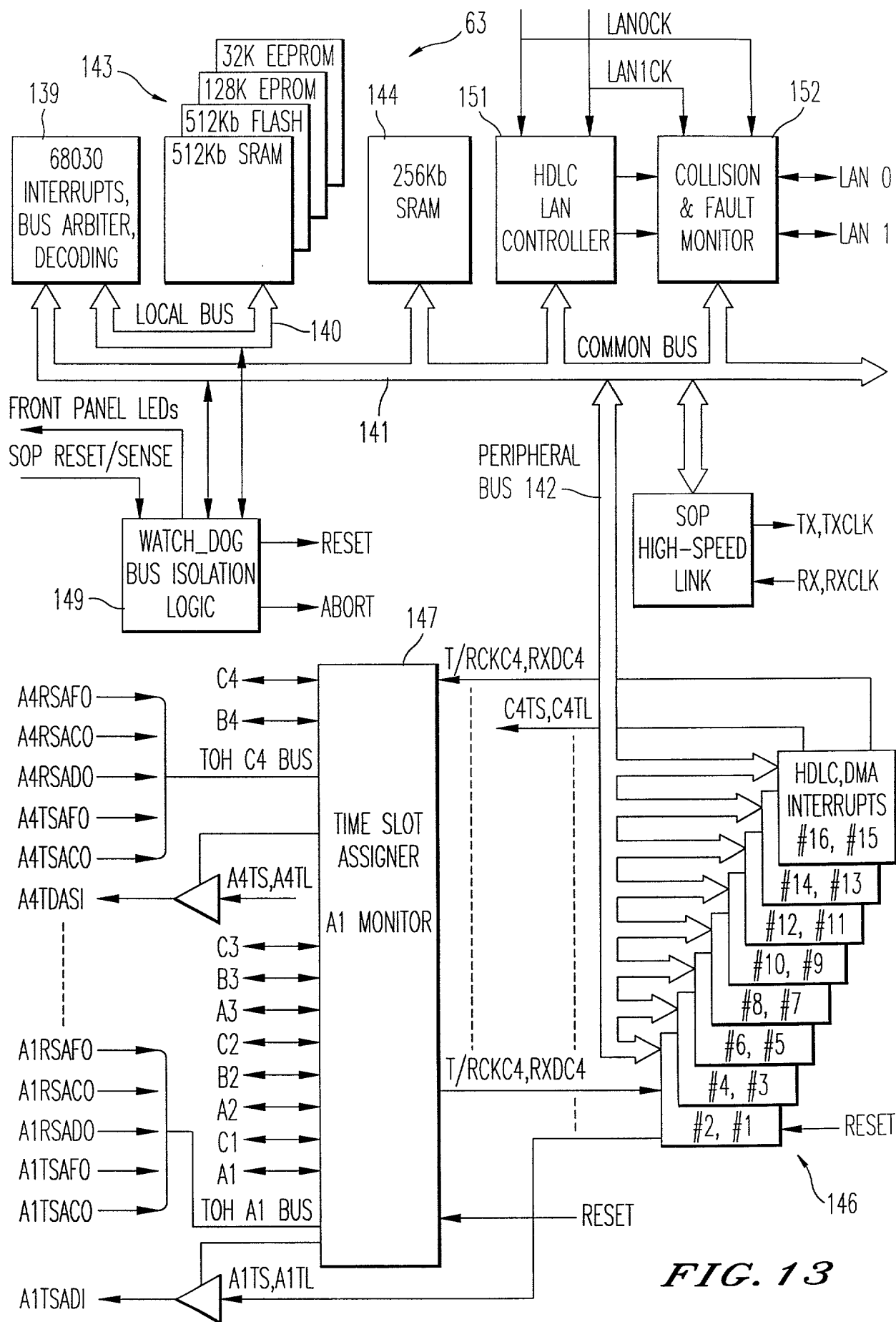
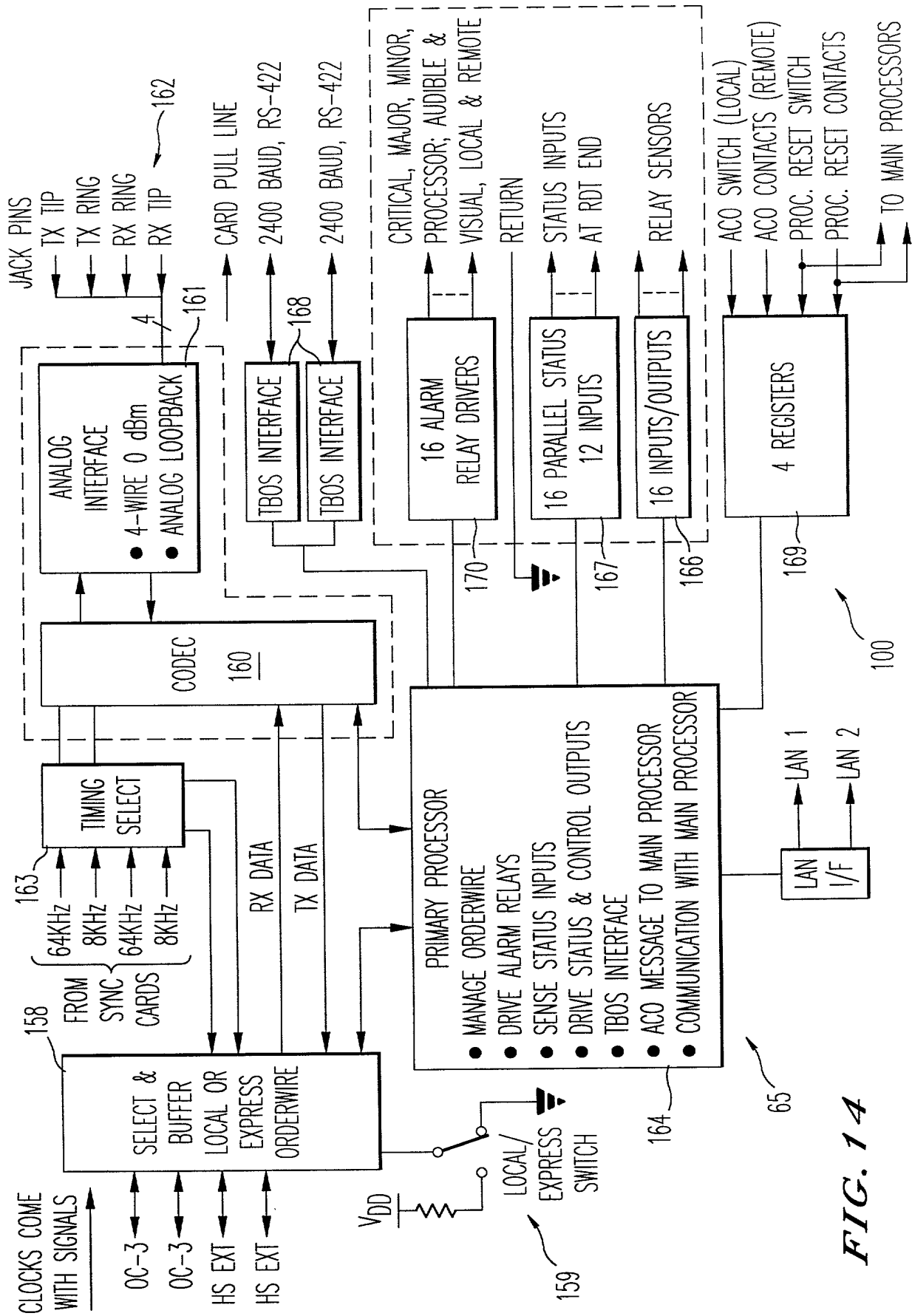


FIG. 13



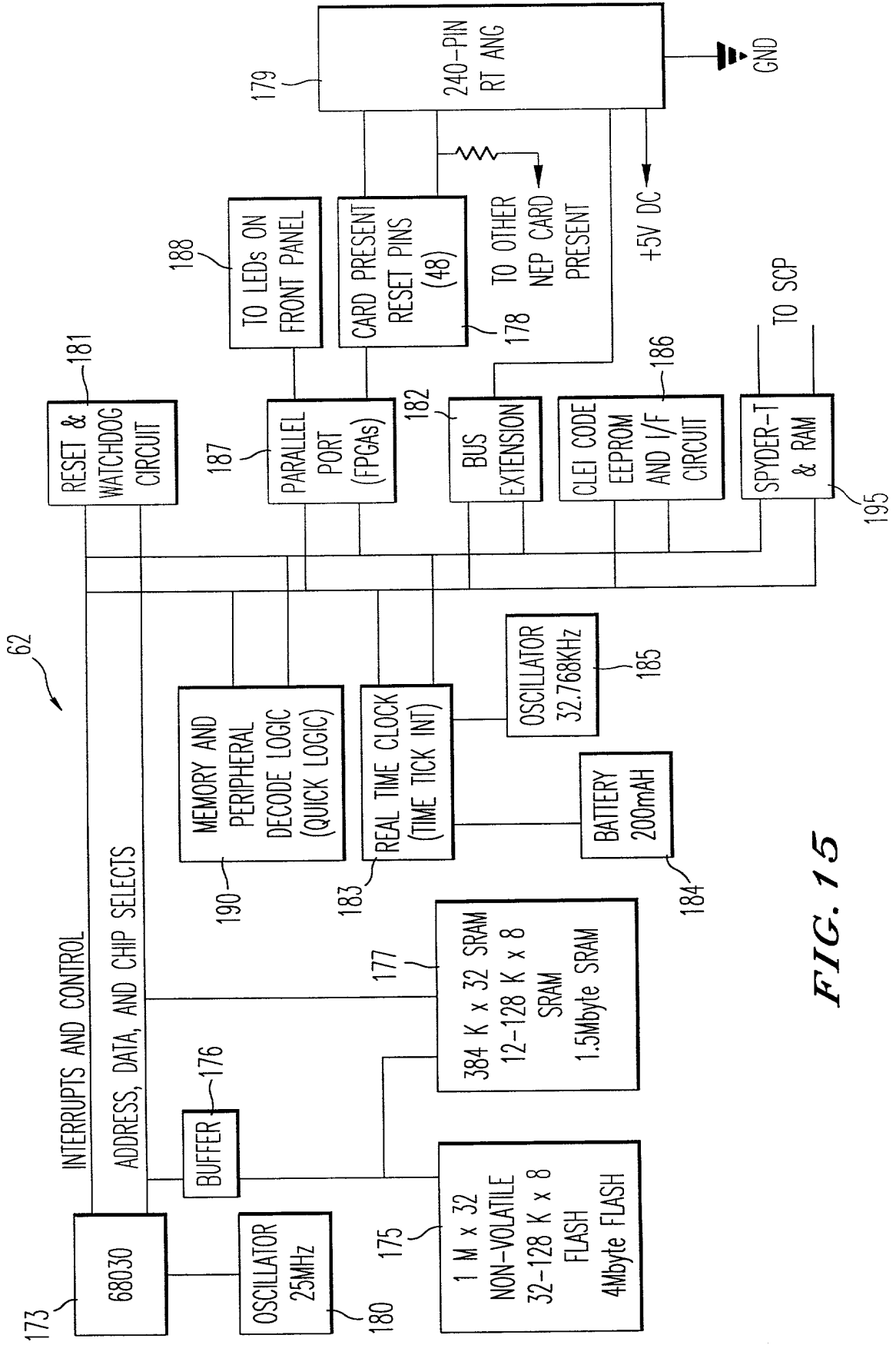


FIG. 15

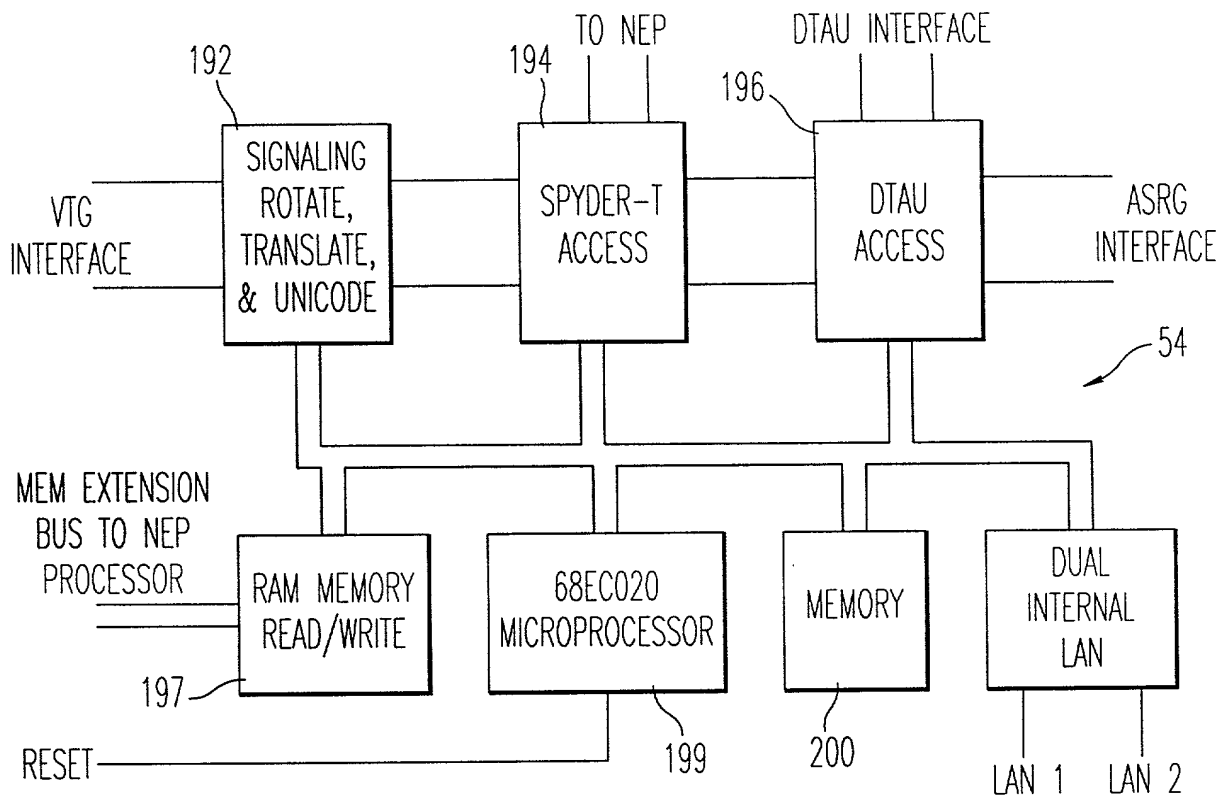


FIG. 16

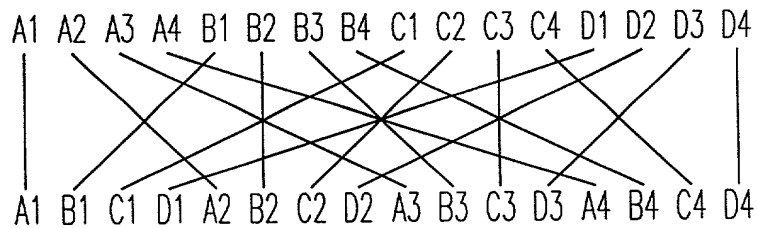


FIG. 17A

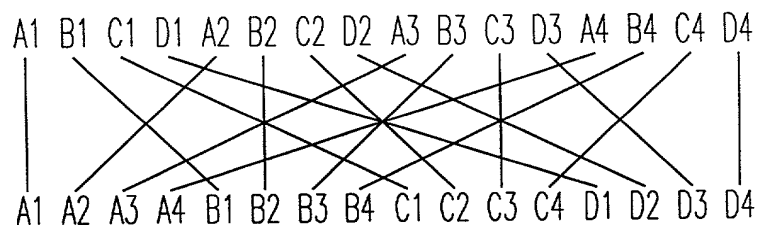


FIG. 17B

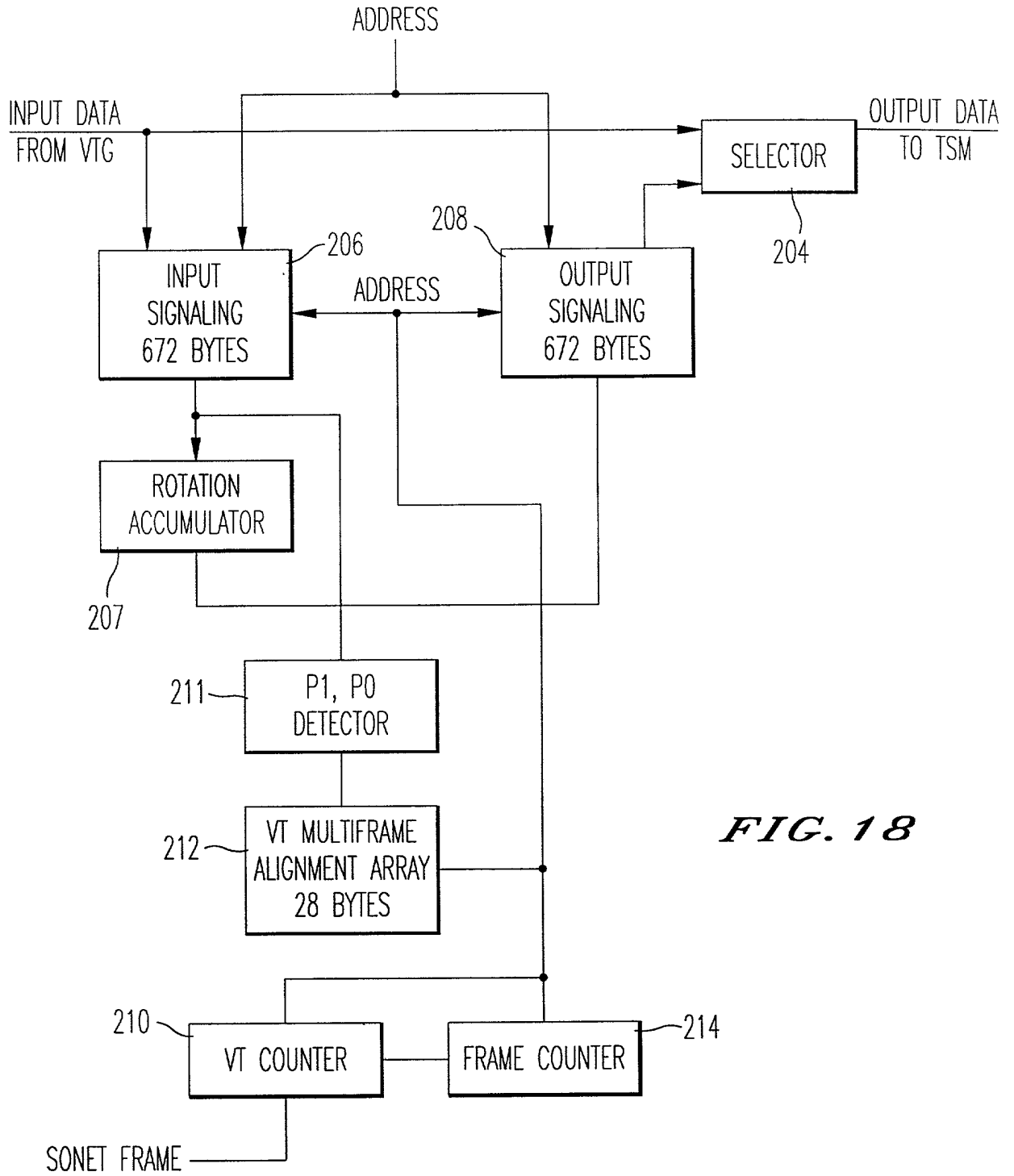


FIG. 18

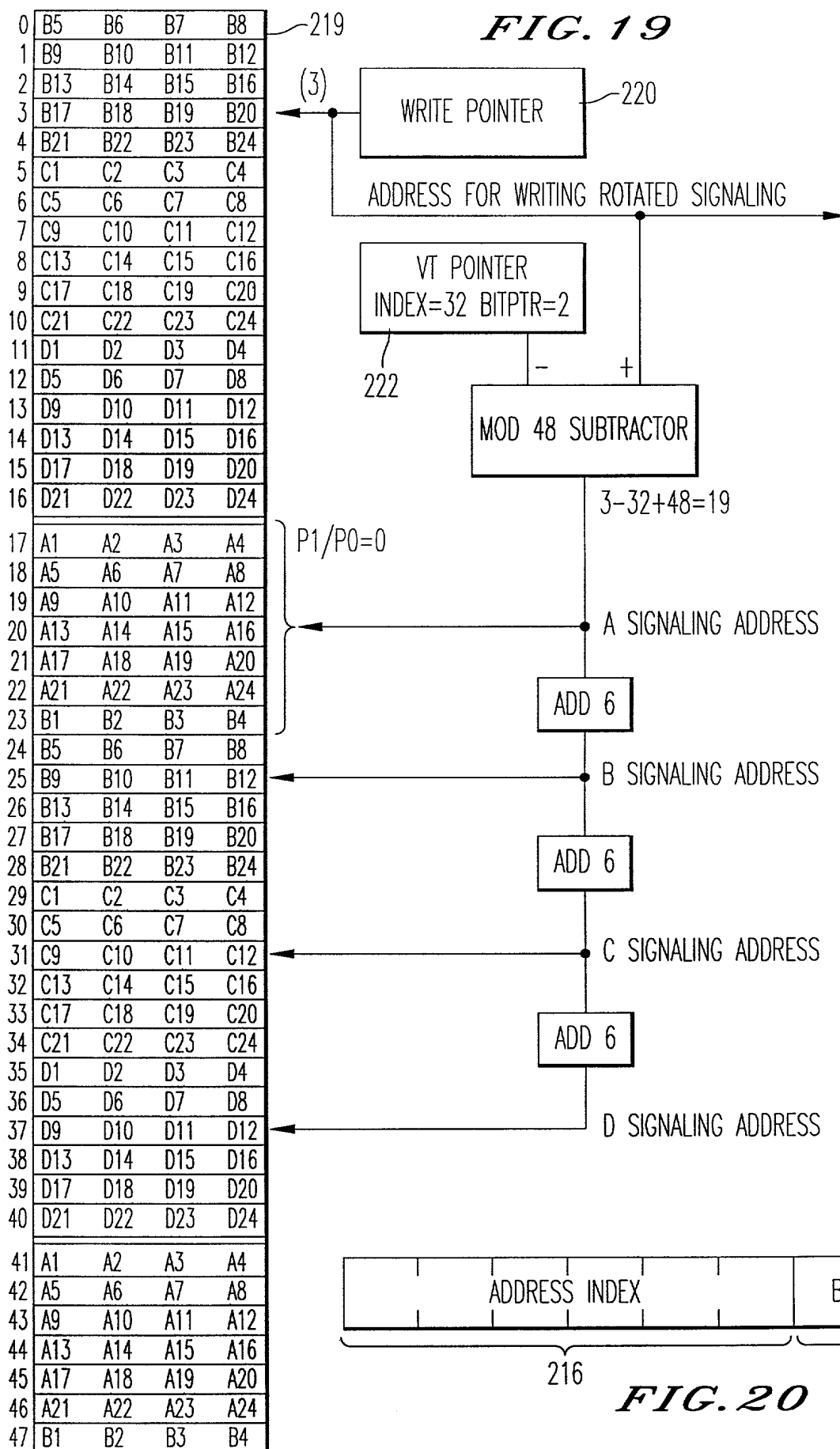
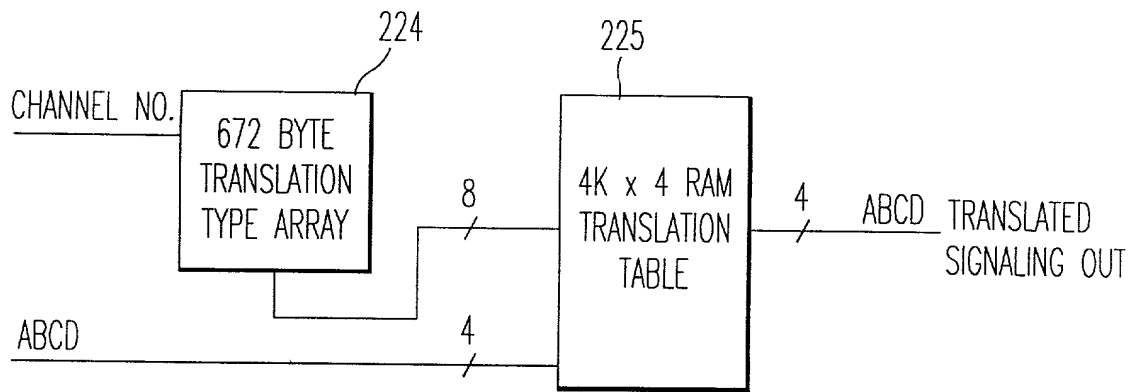


FIG. 20



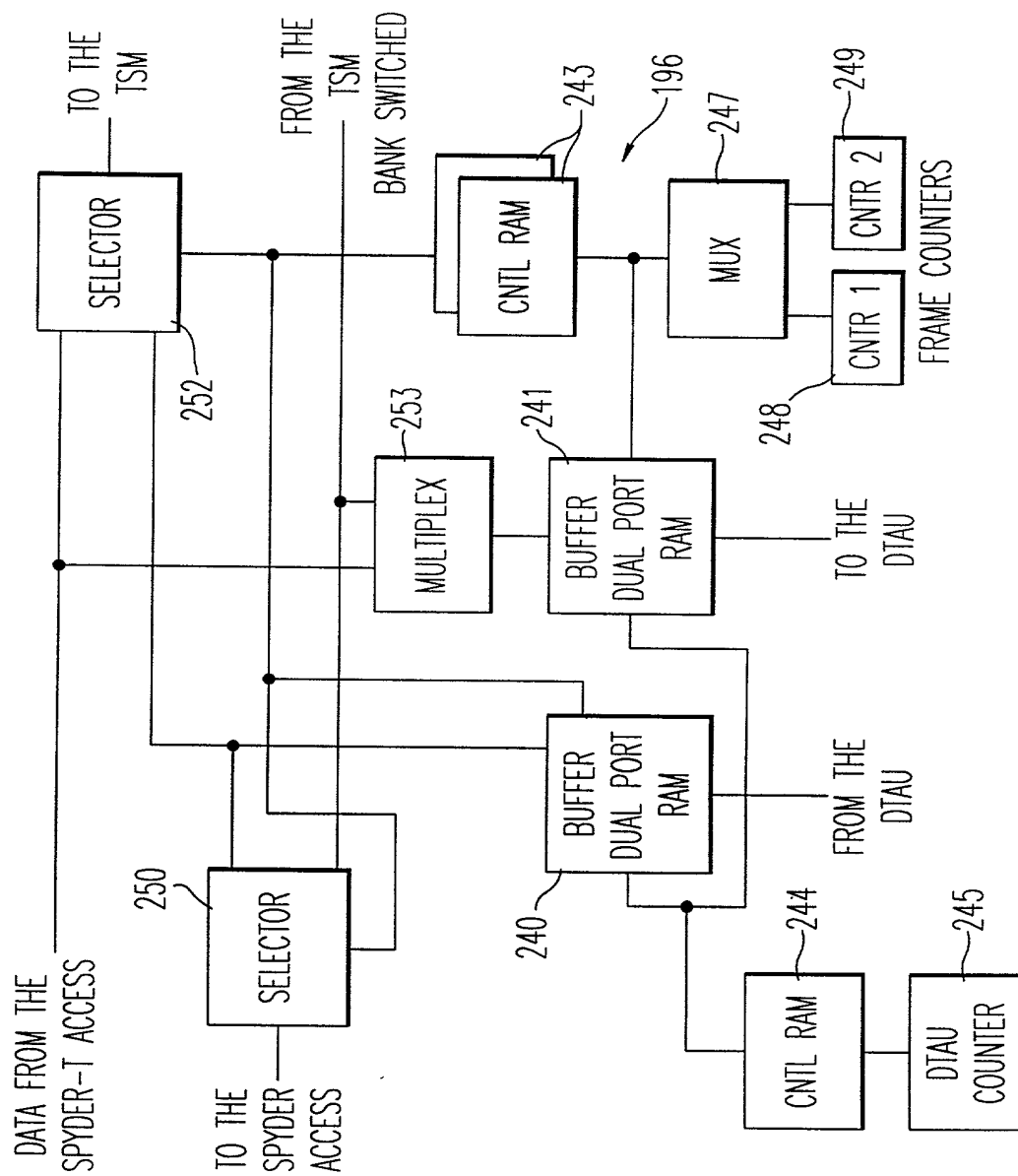


FIG. 24

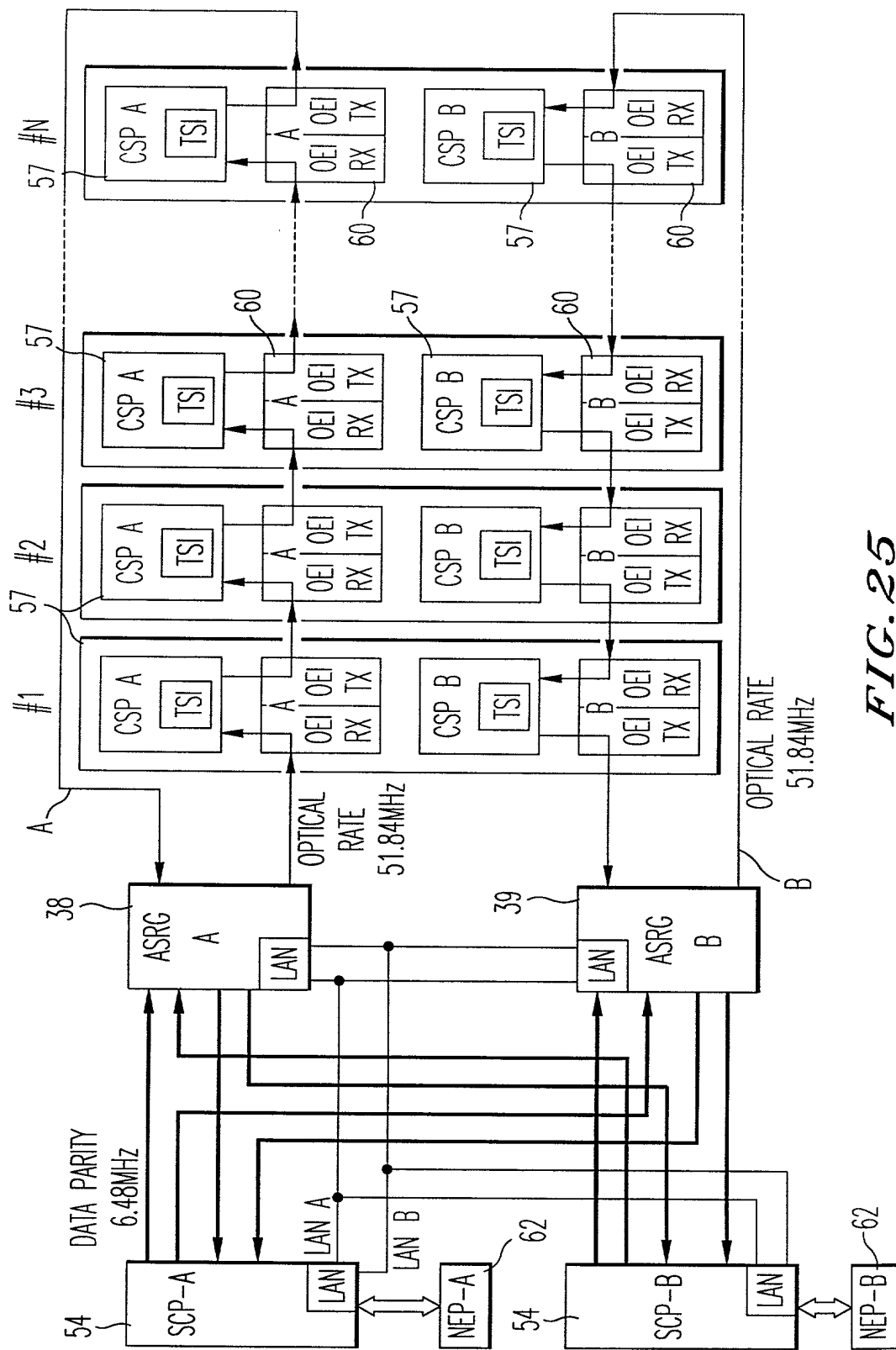


FIG. 25

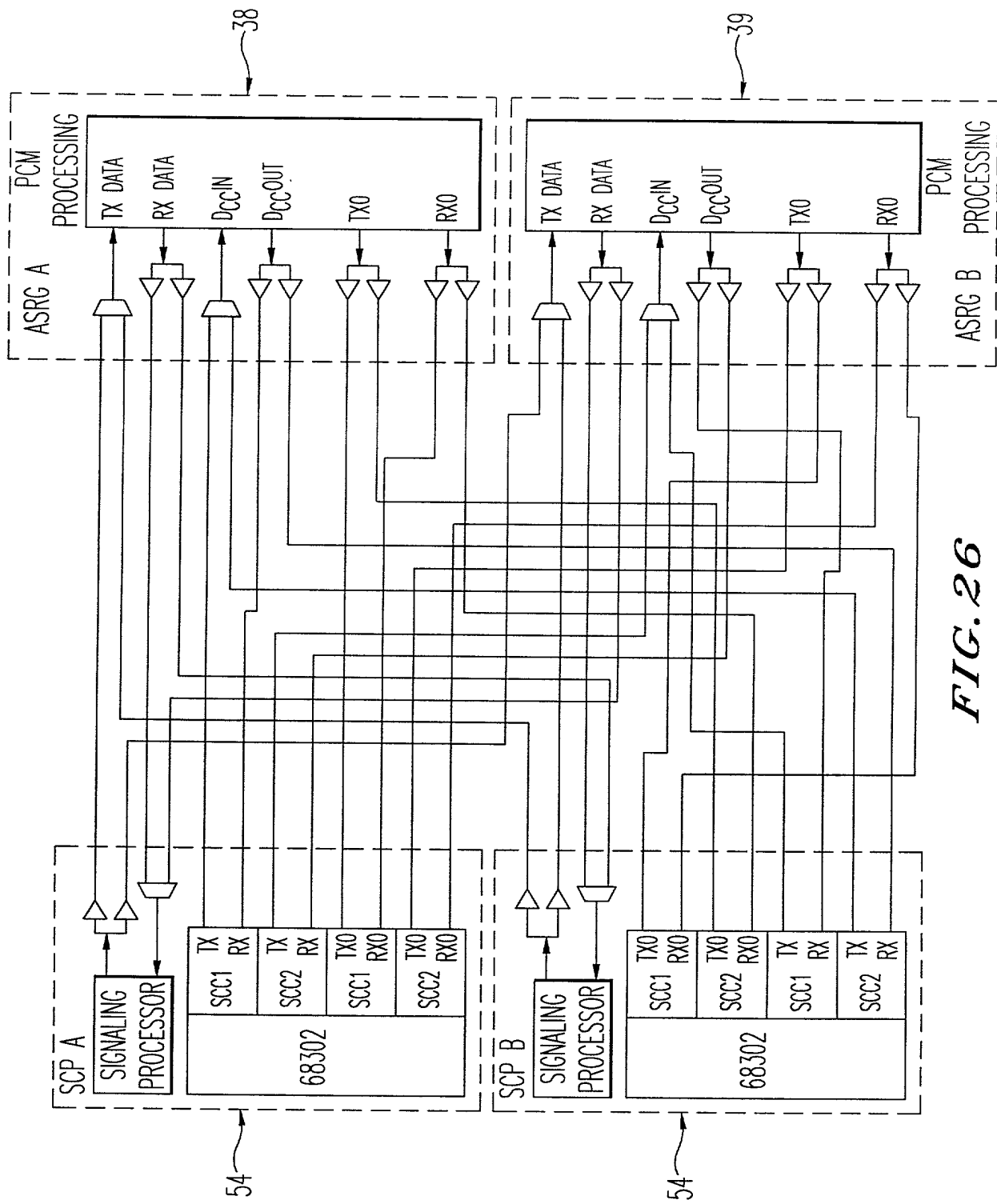
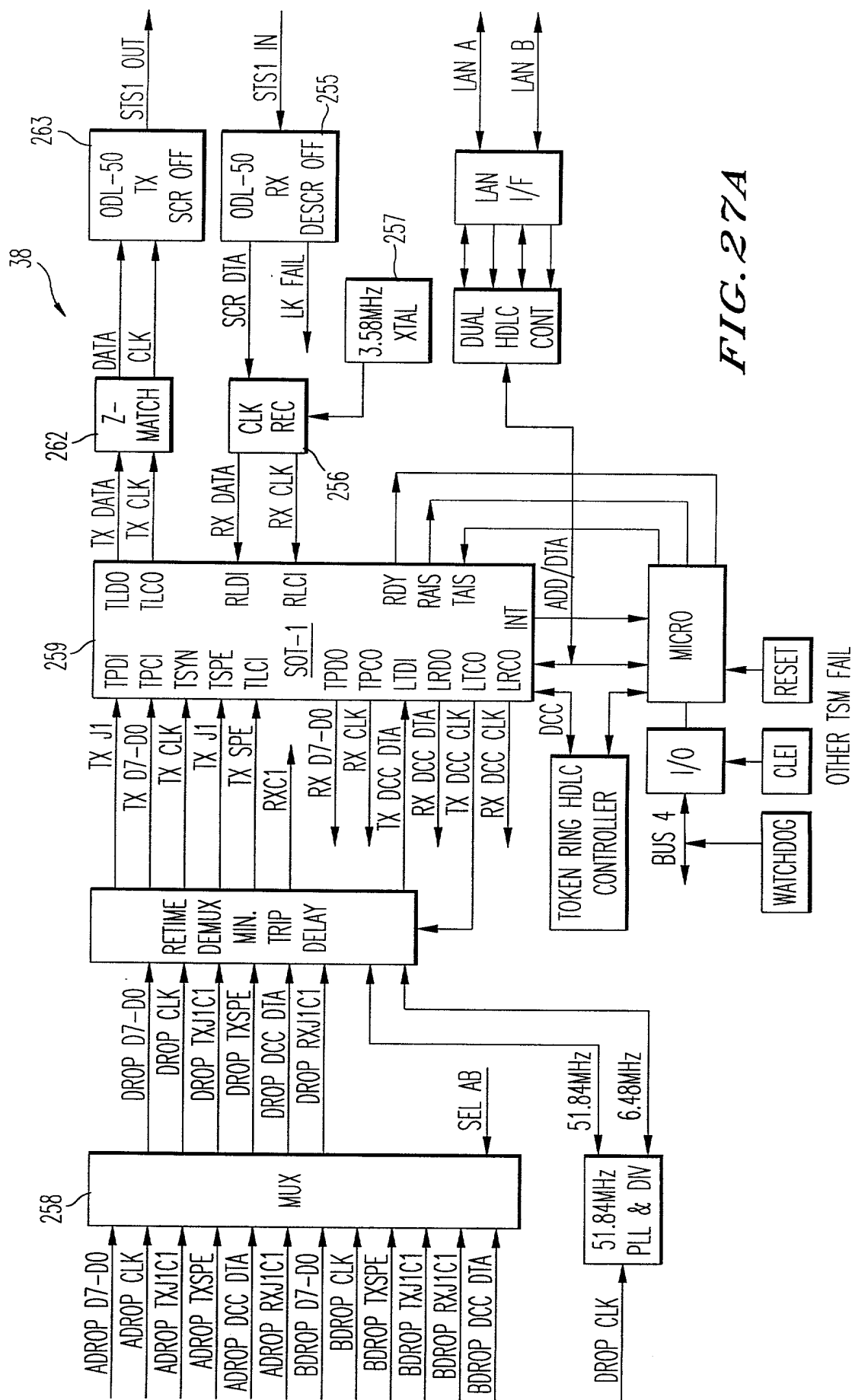


FIG. 26



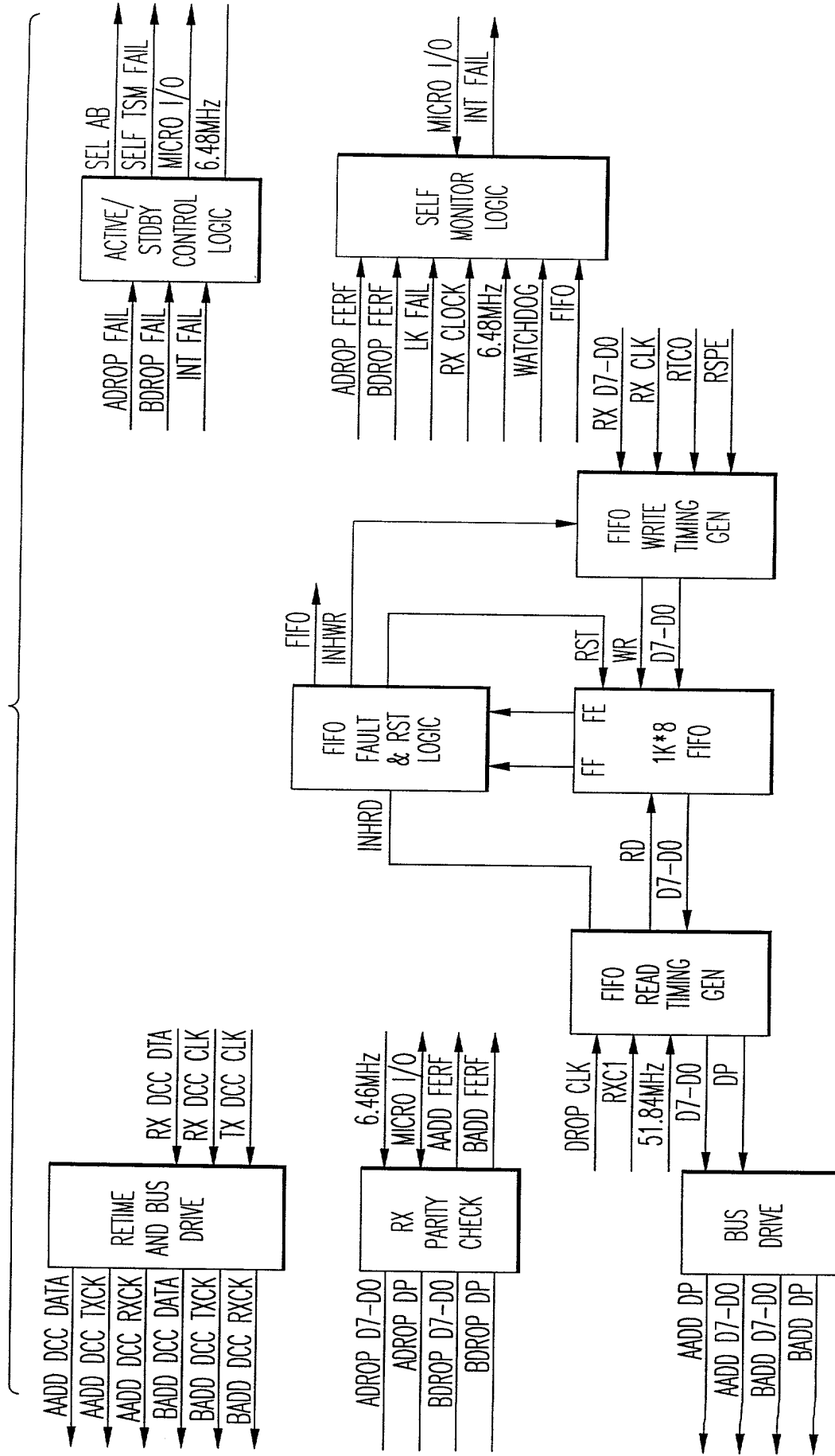


FIG. 27B

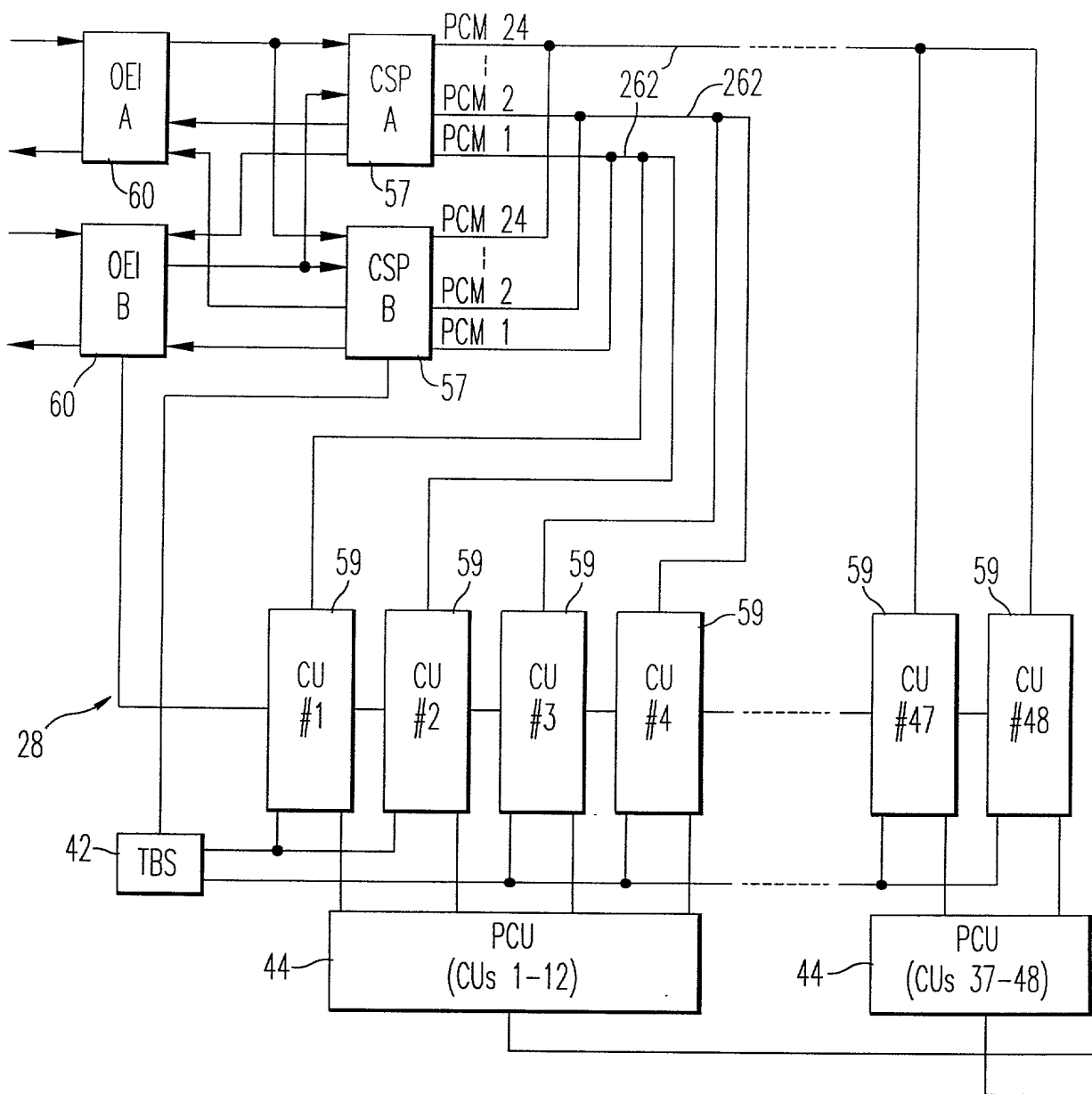


FIG. 28

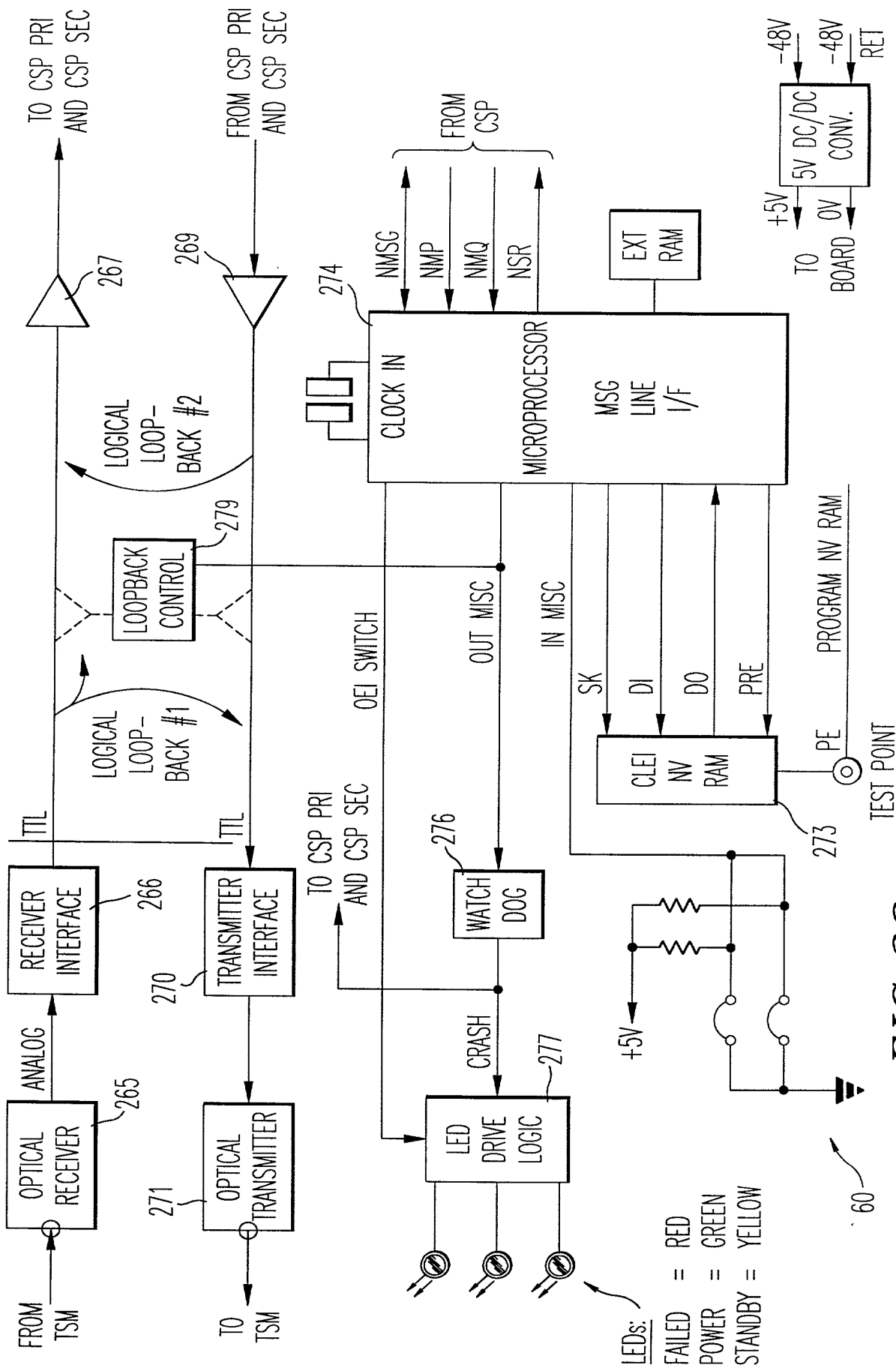
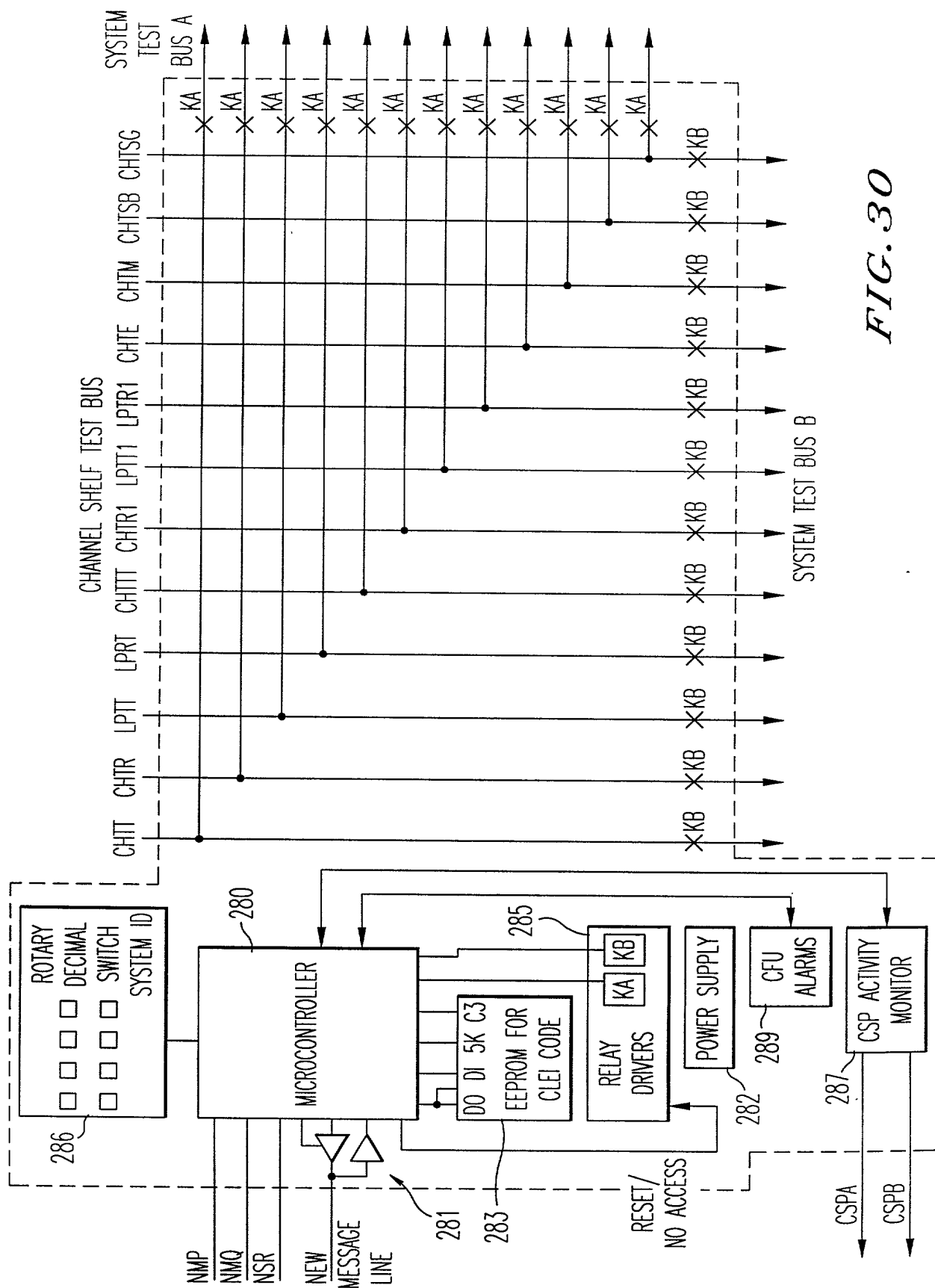


FIG. 29



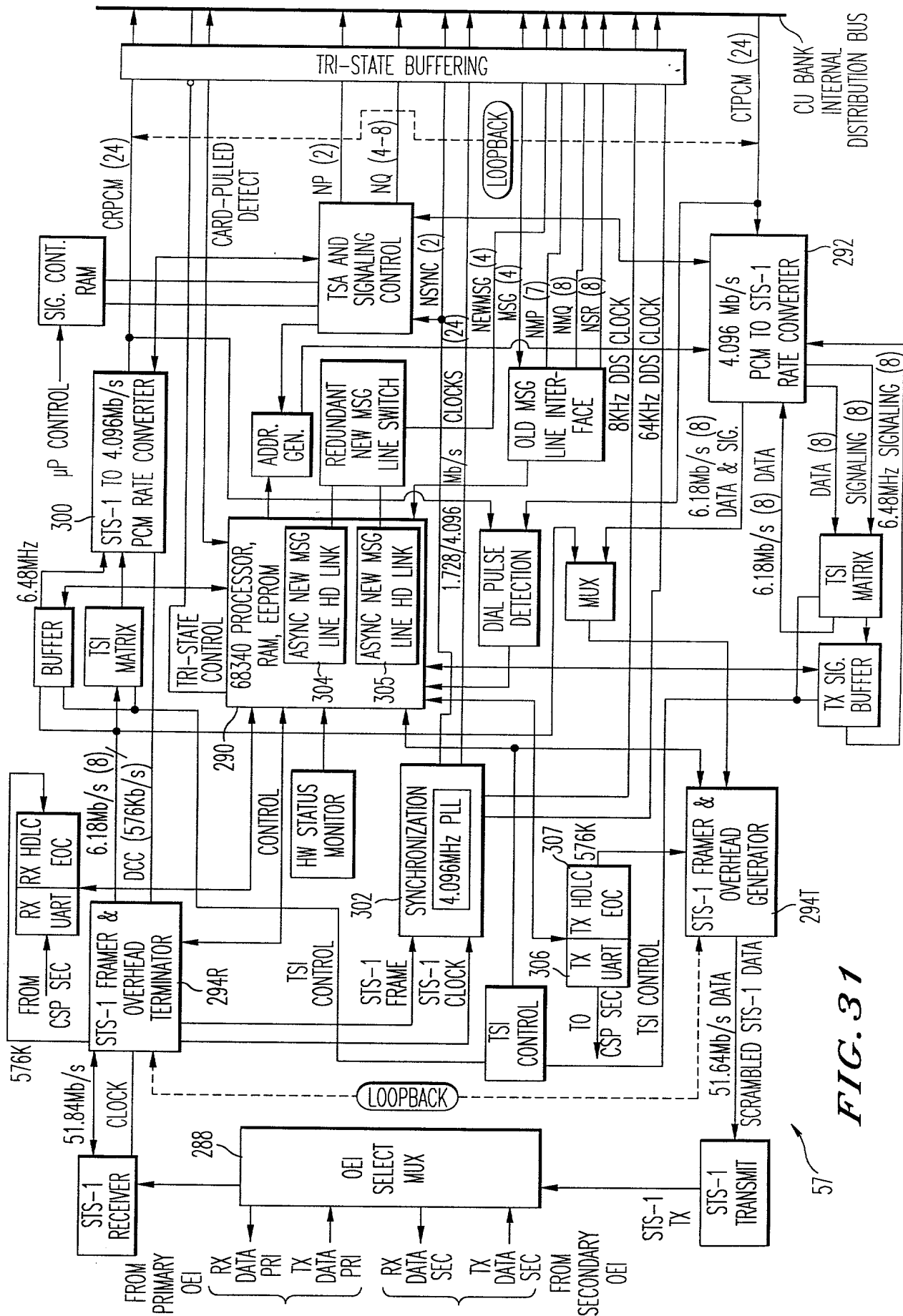


FIG. 31

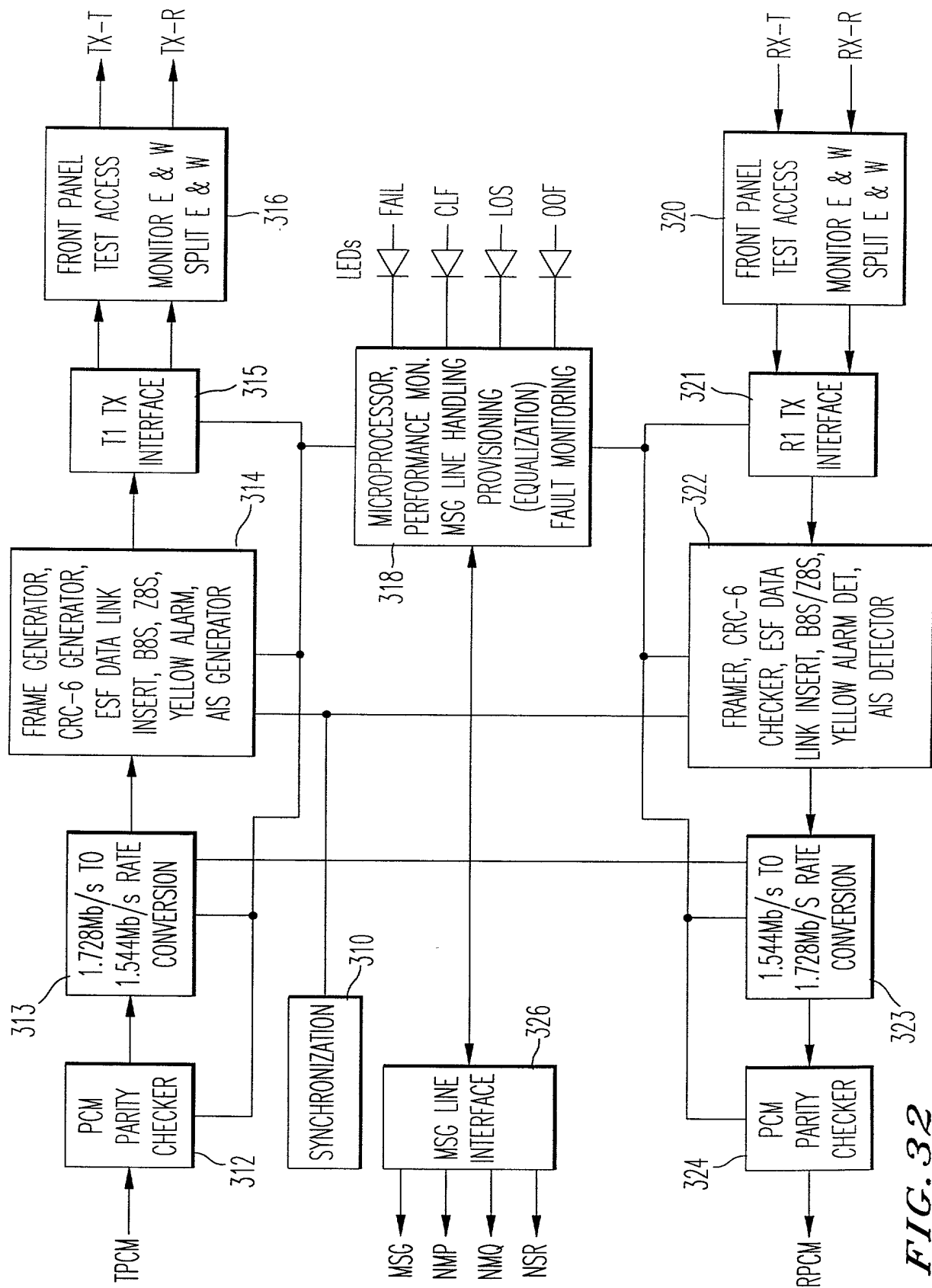


FIG. 32

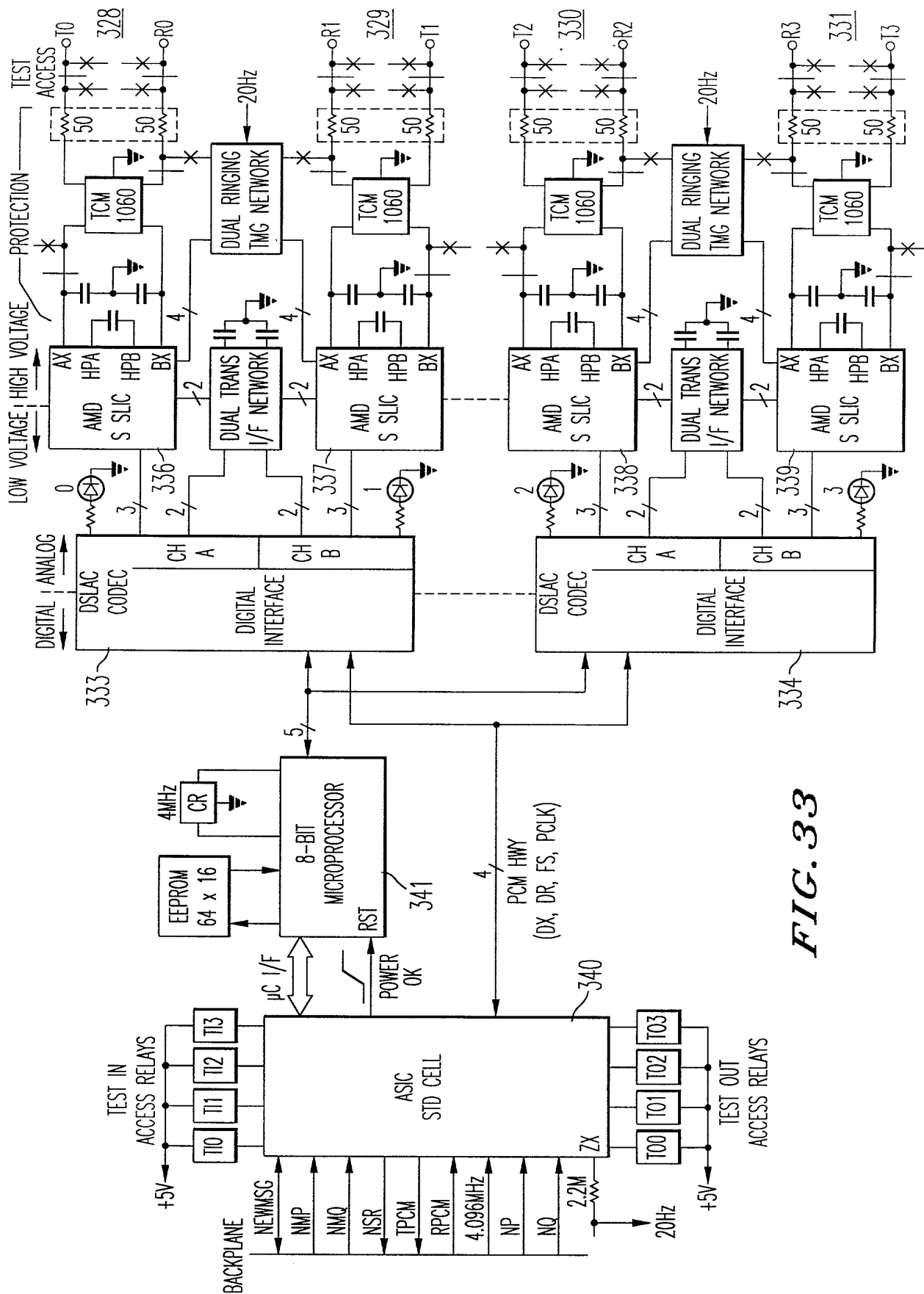


FIG. 33

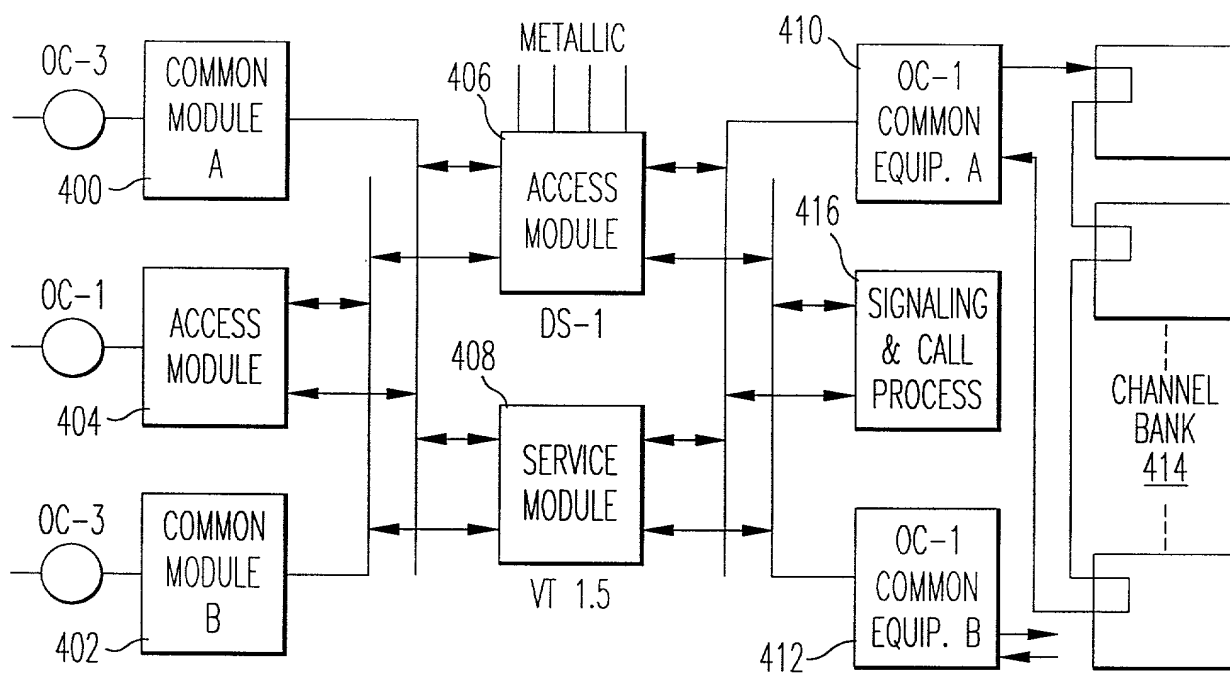


FIG. 34

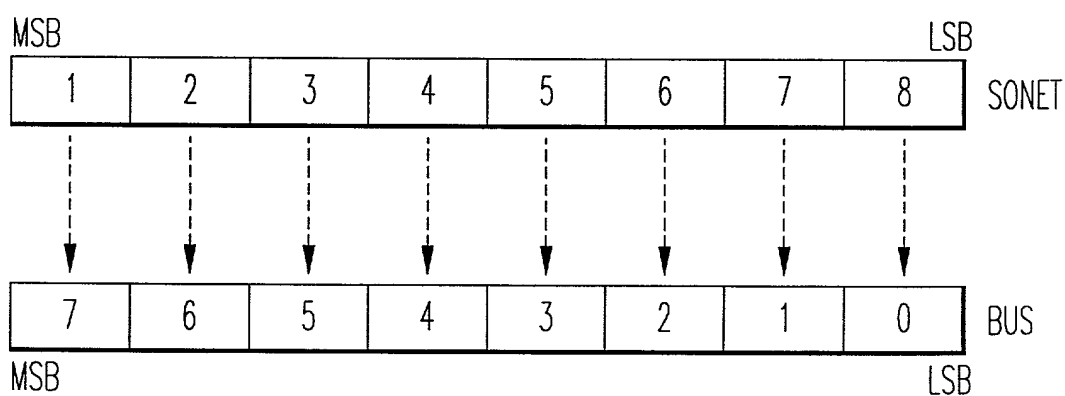
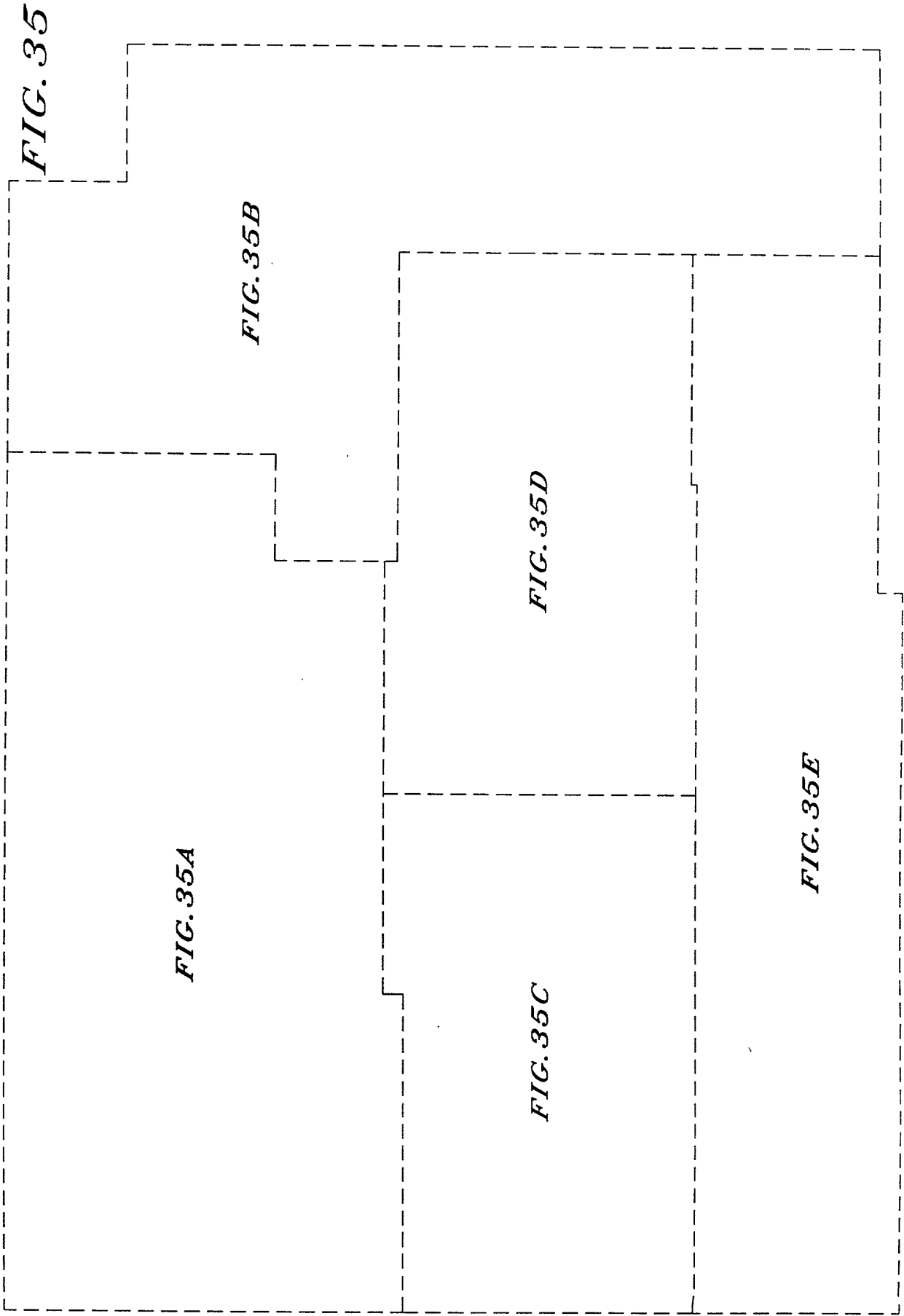
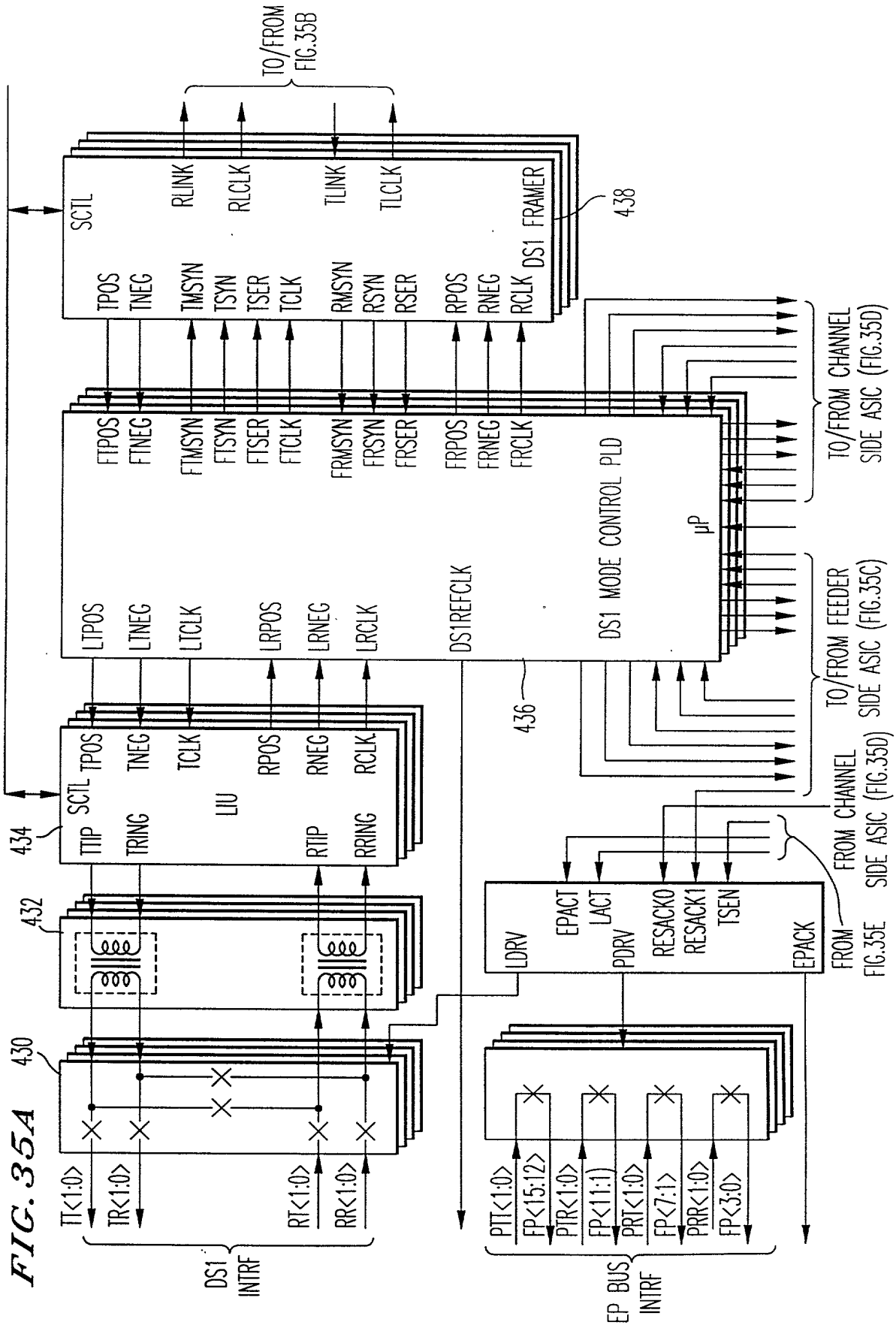


FIG. 37





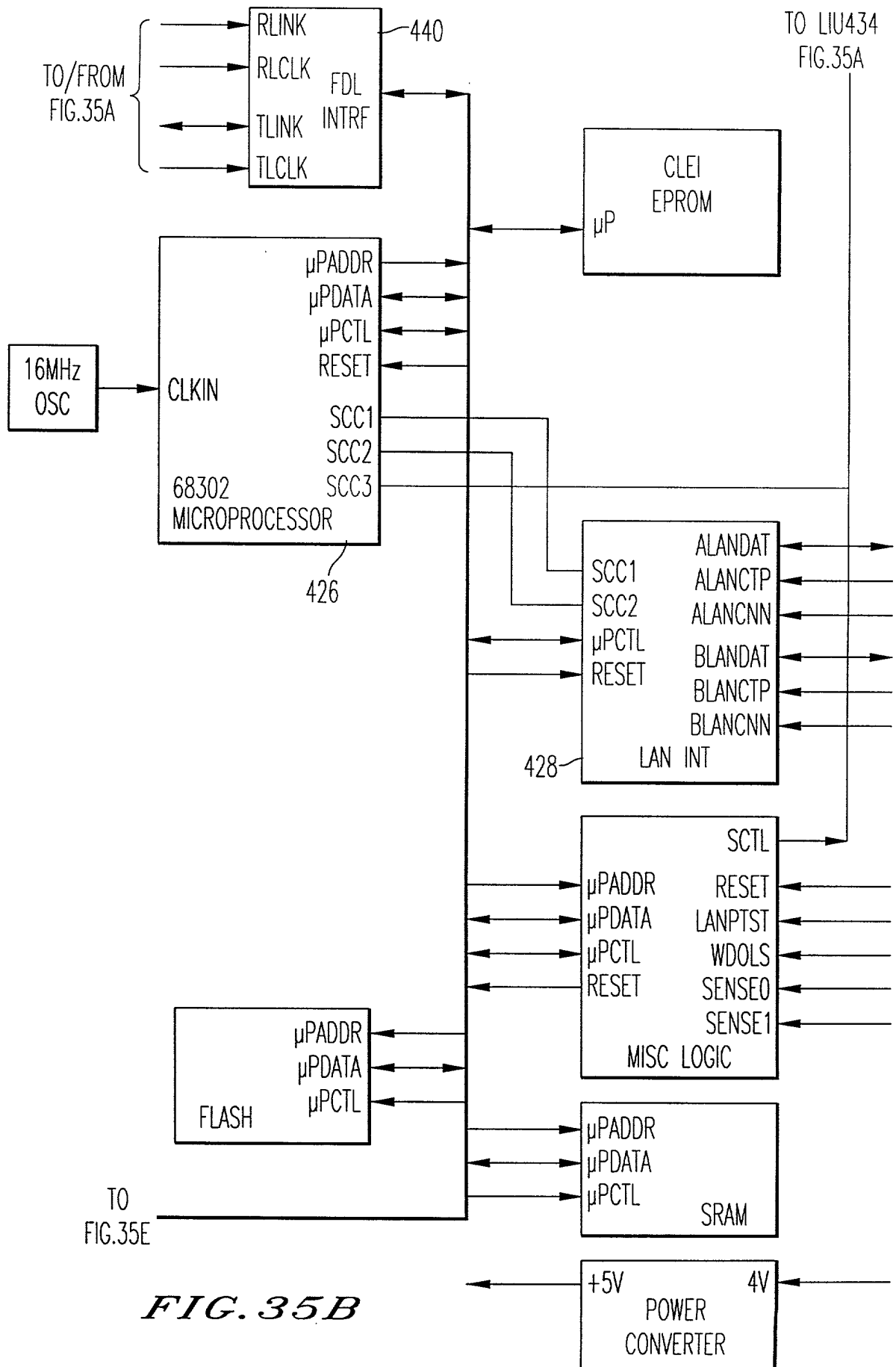


FIG. 35B

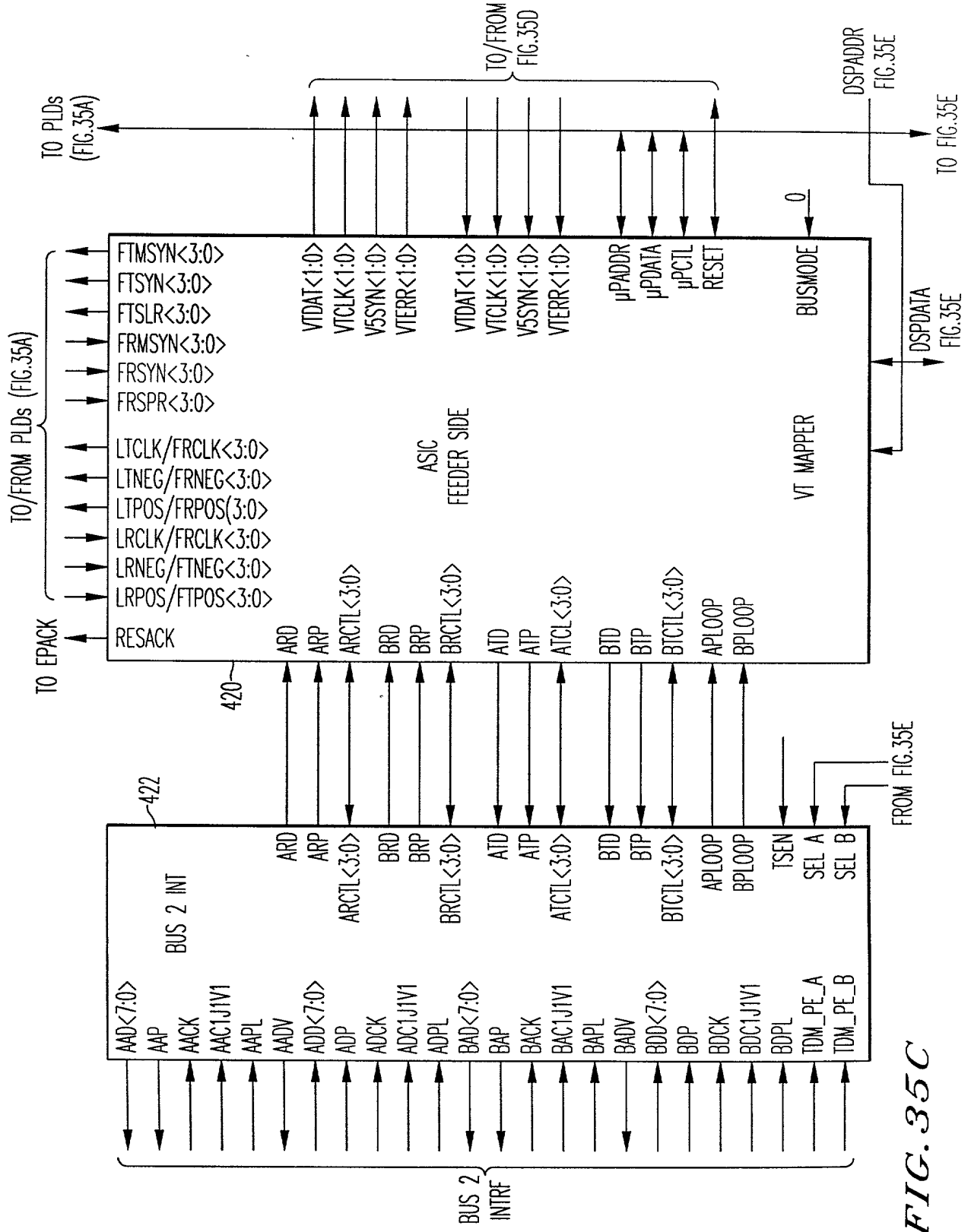
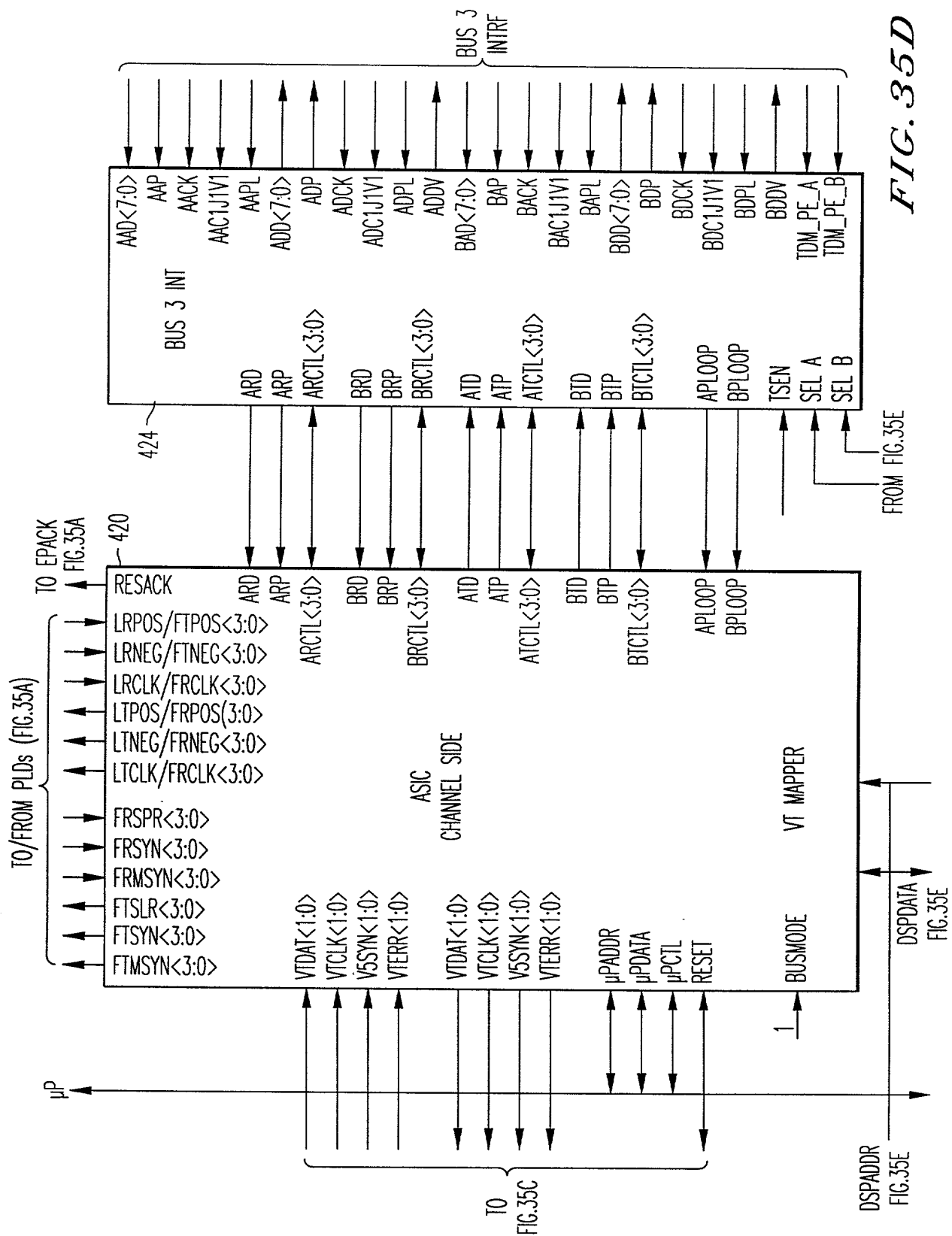


FIG. 35C



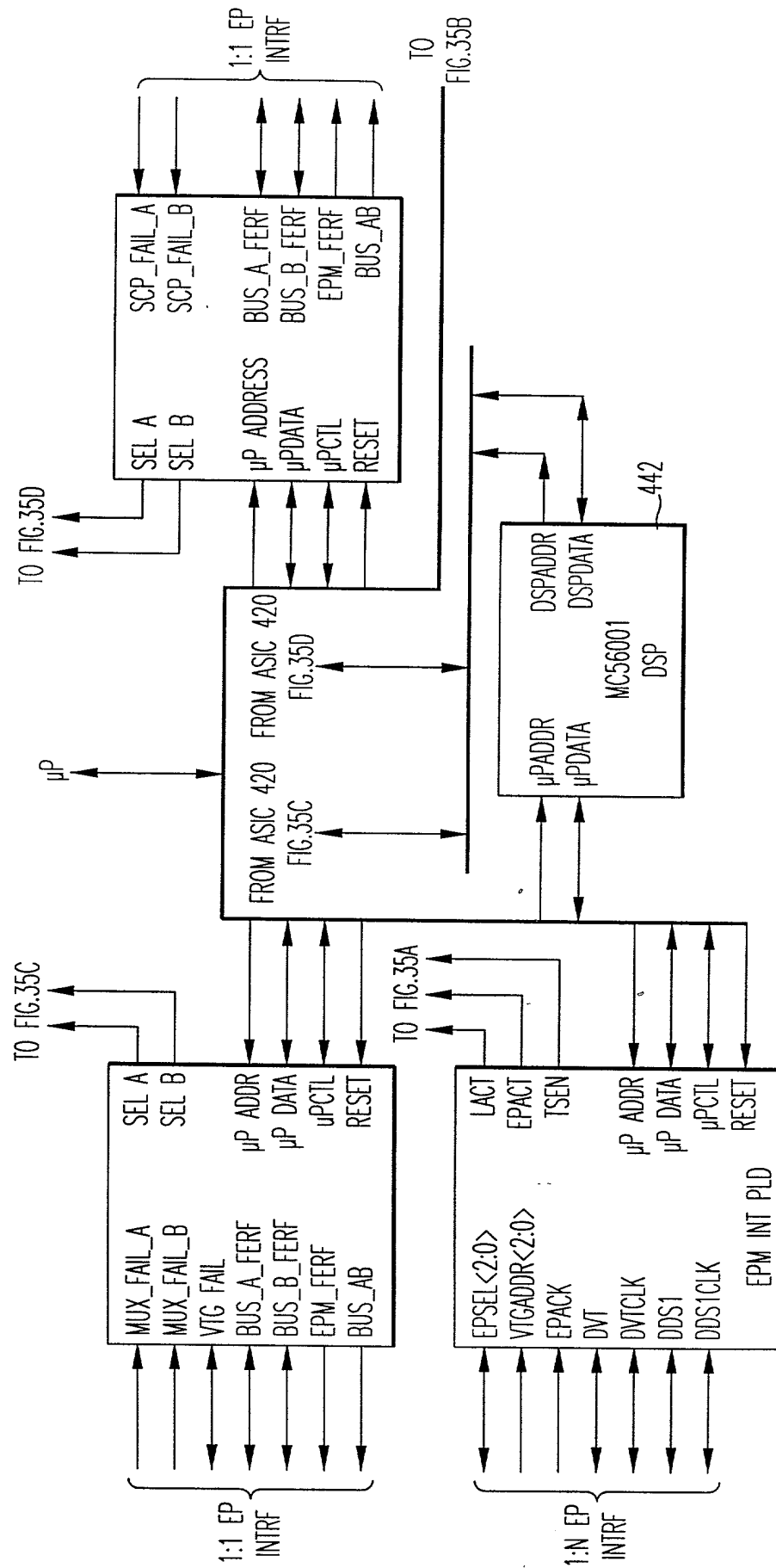


FIG. 35E

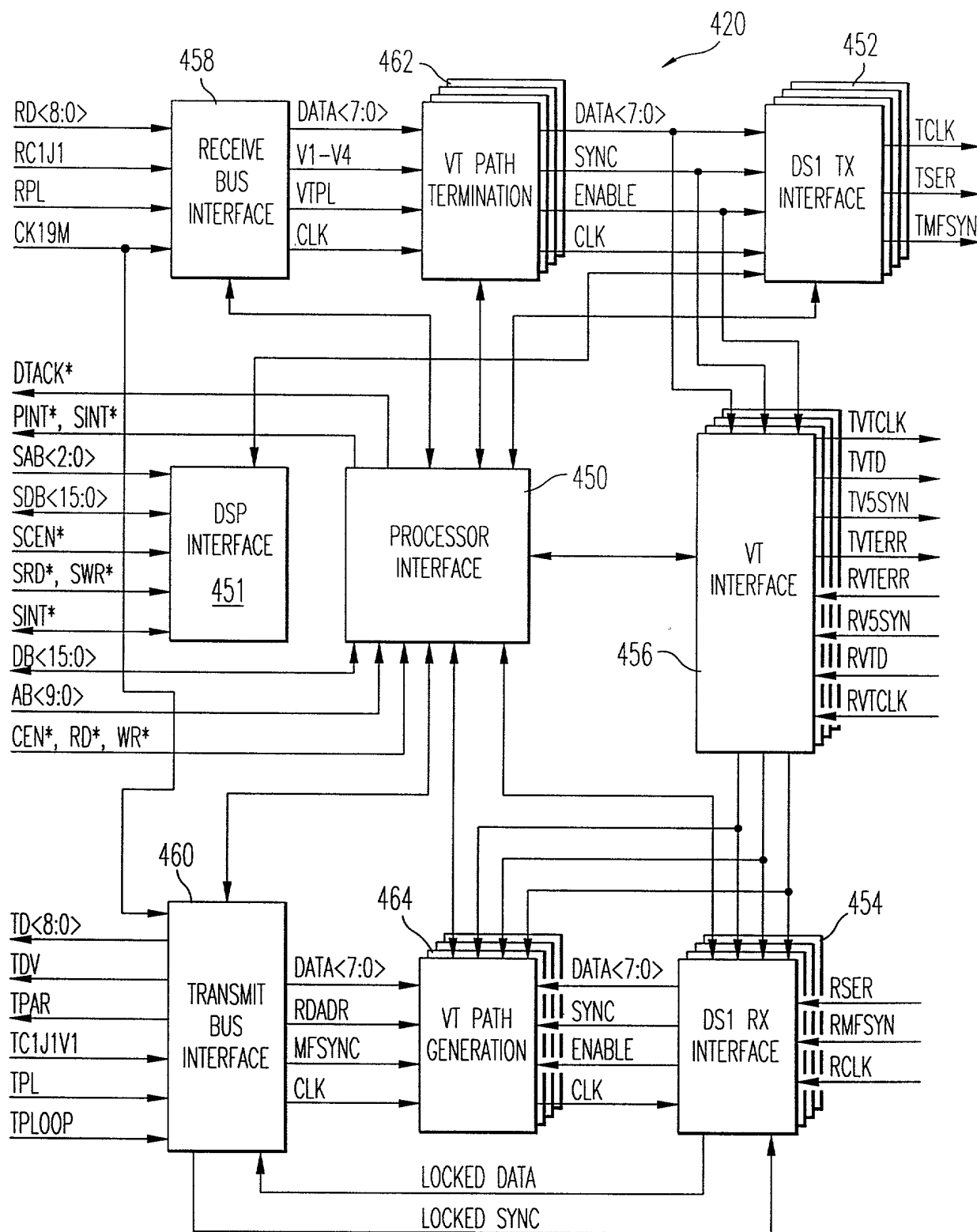


FIG. 36

FIG. 38

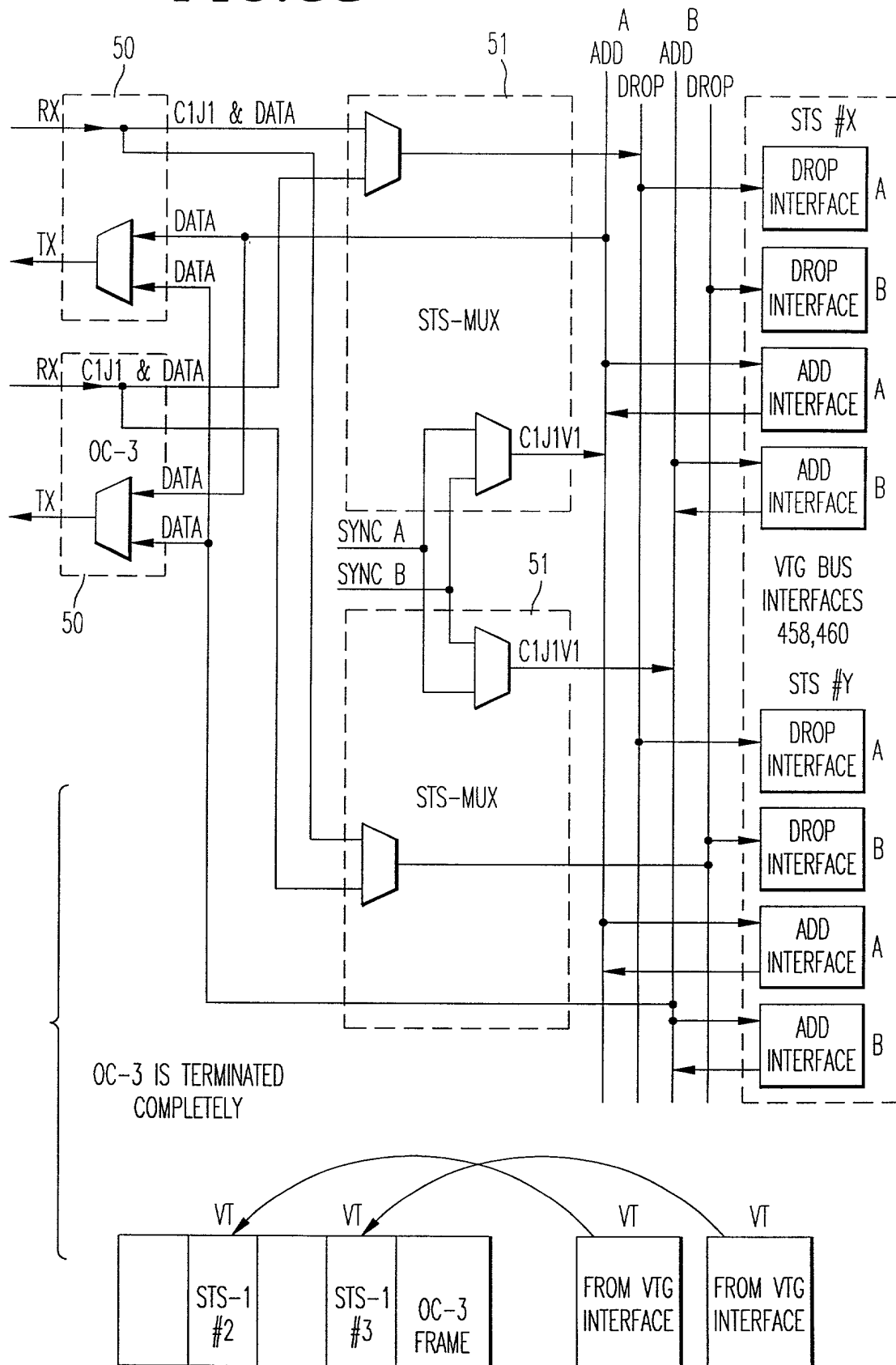


FIG. 39

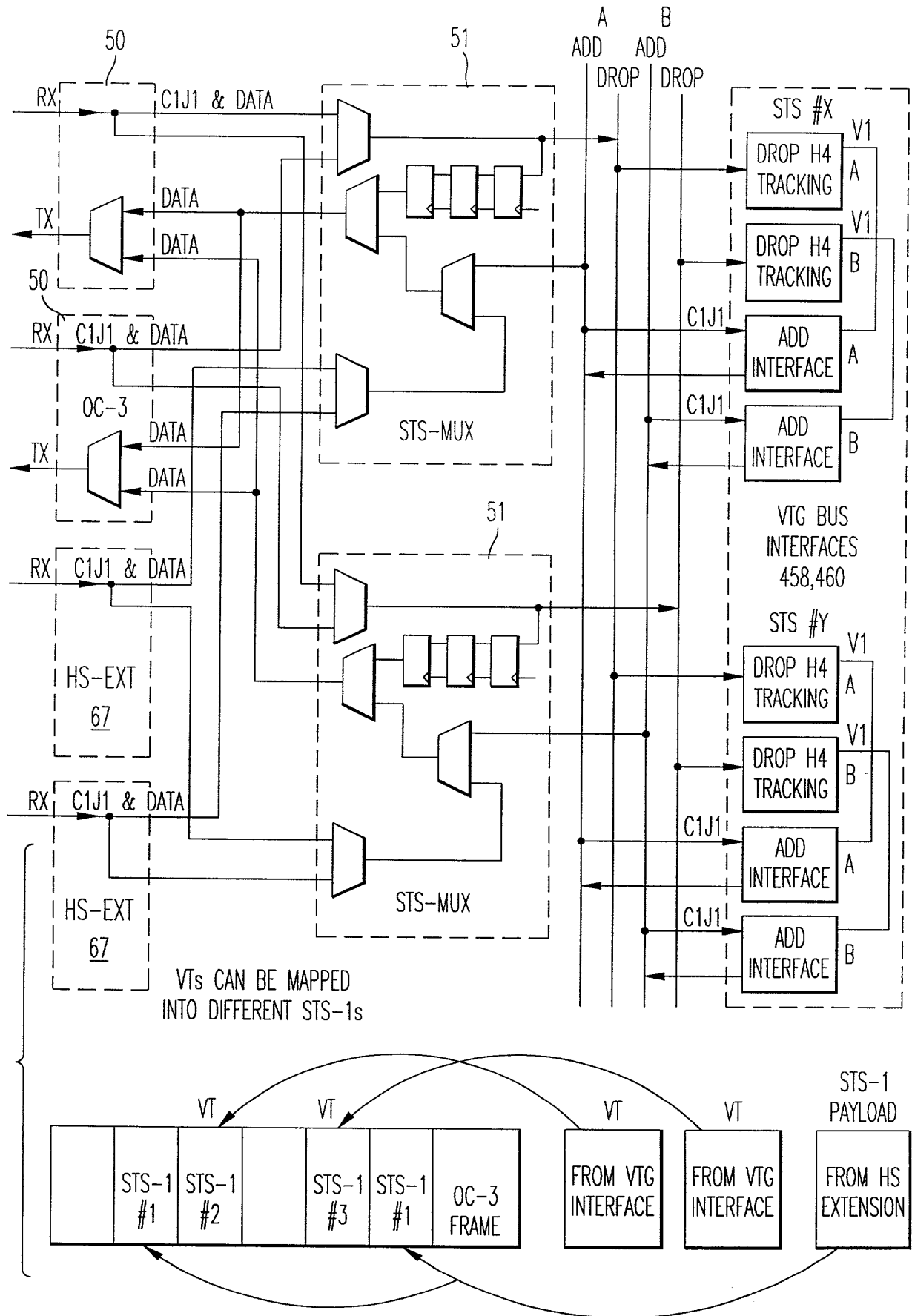


FIG. 40

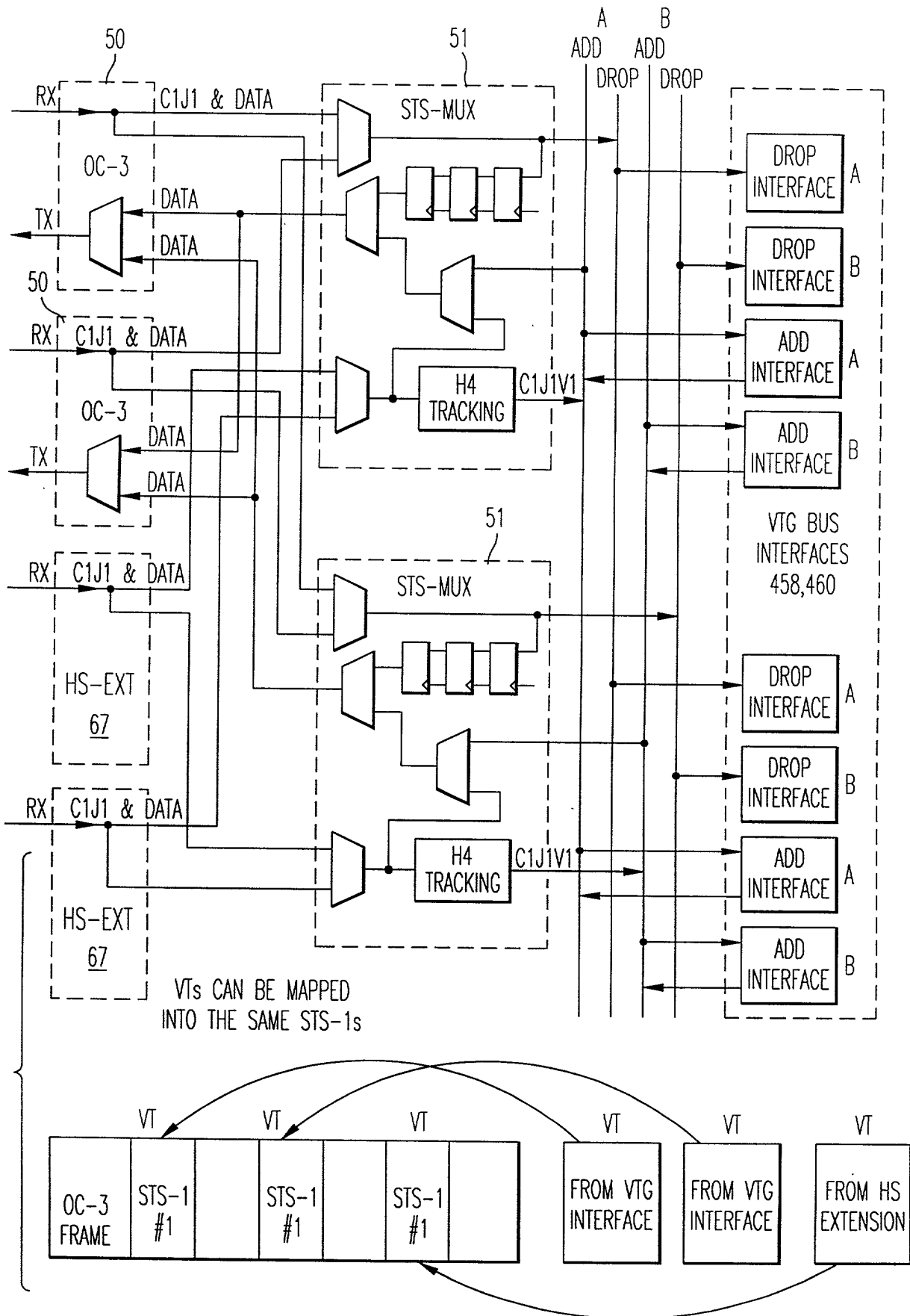
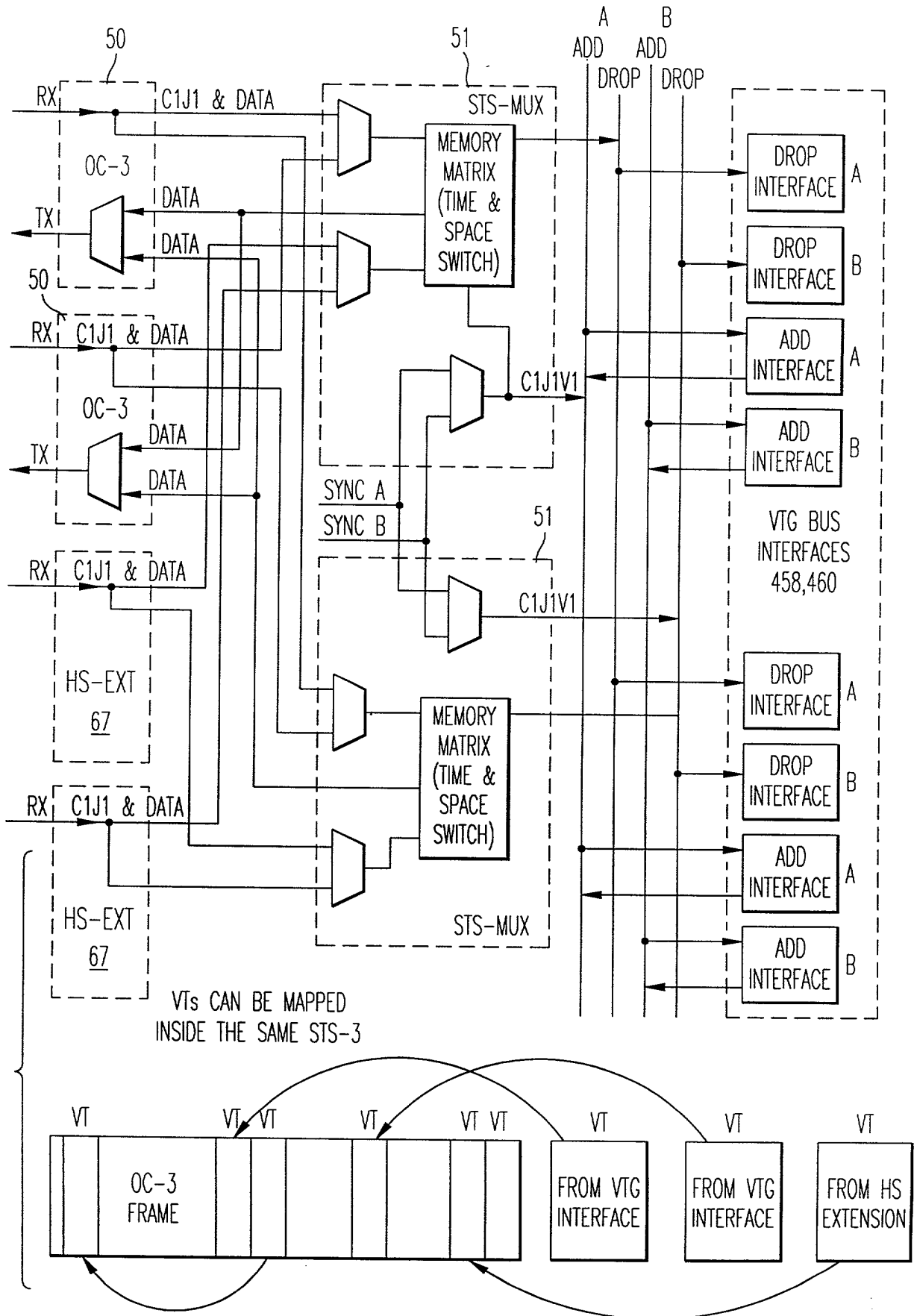


FIG. 41



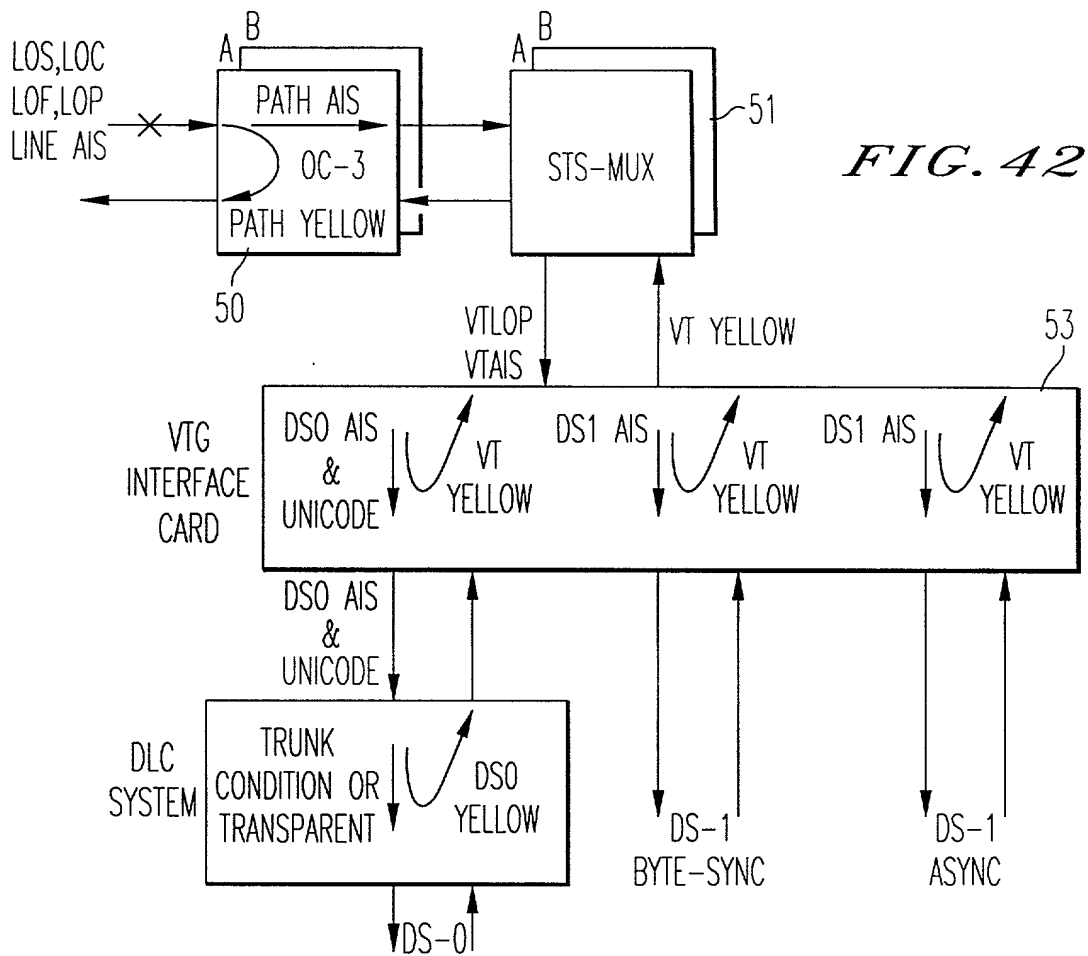


FIG. 42

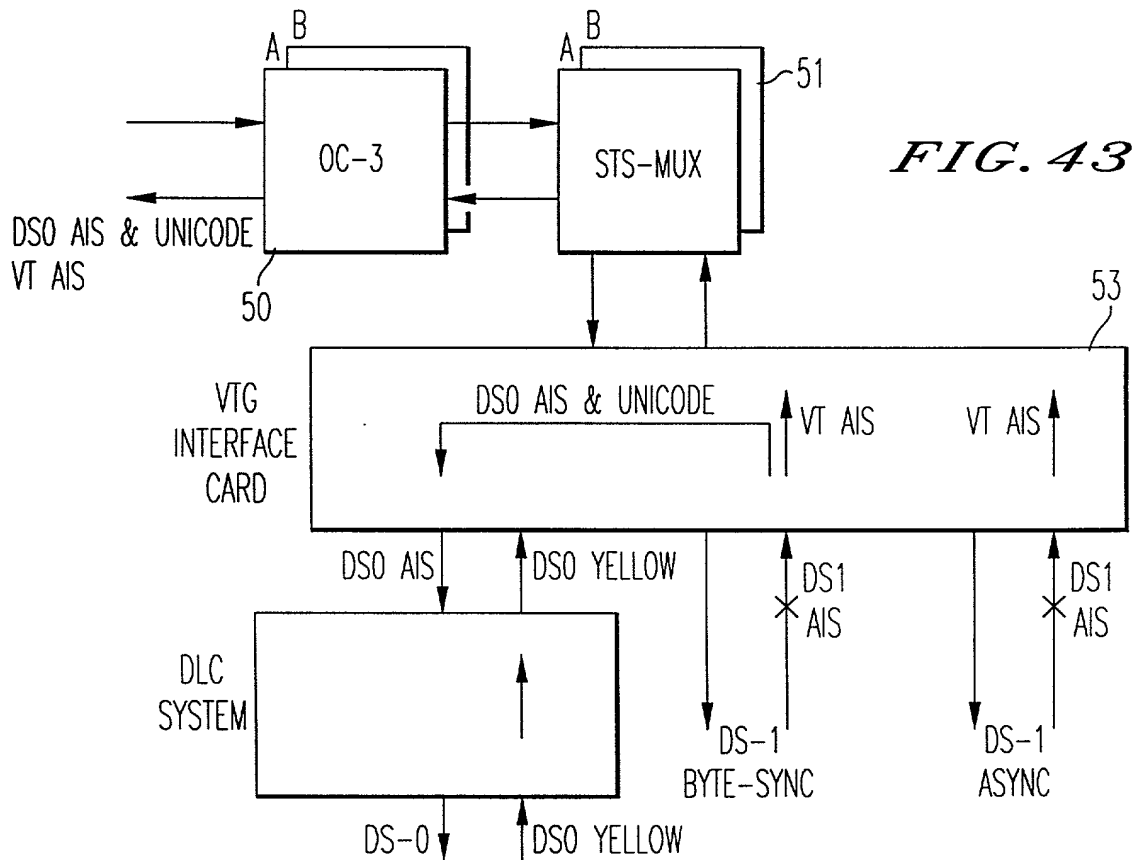
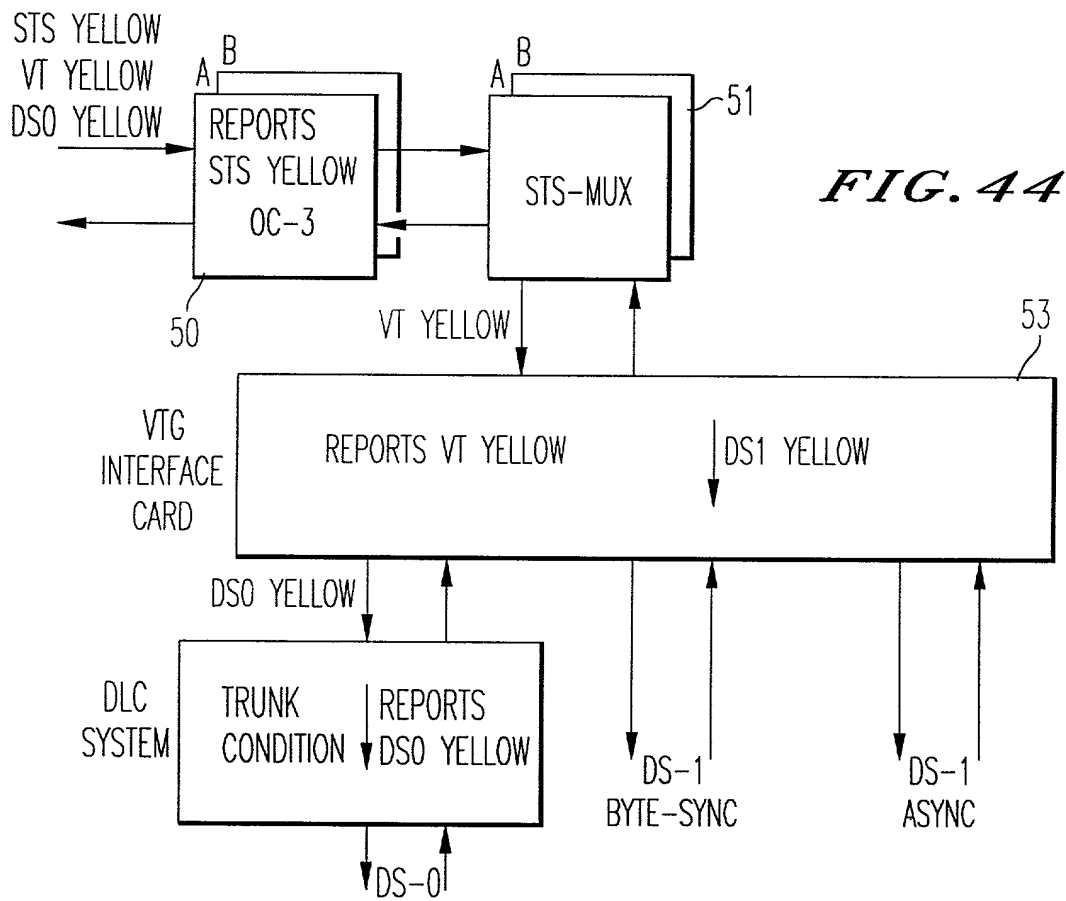
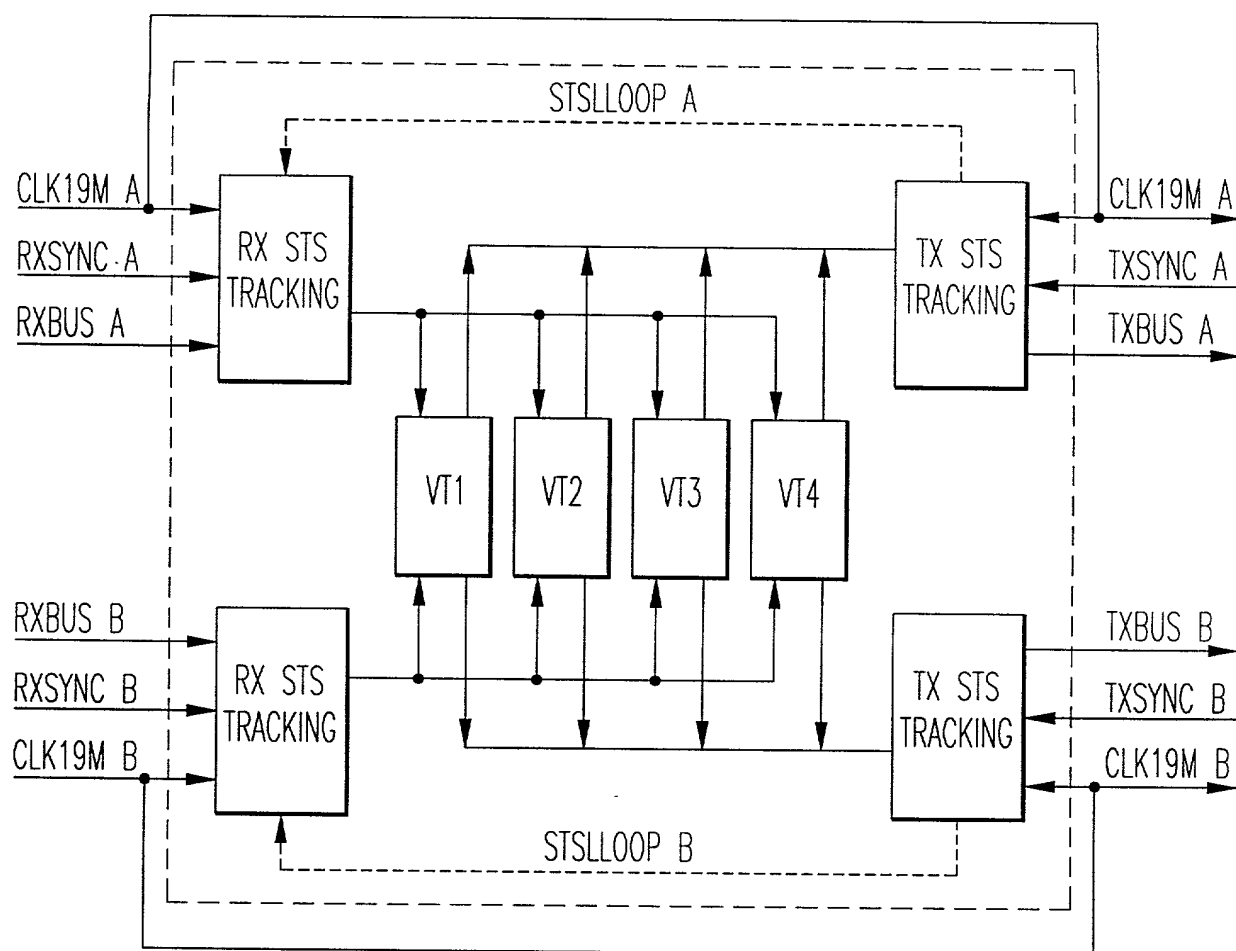


FIG. 43





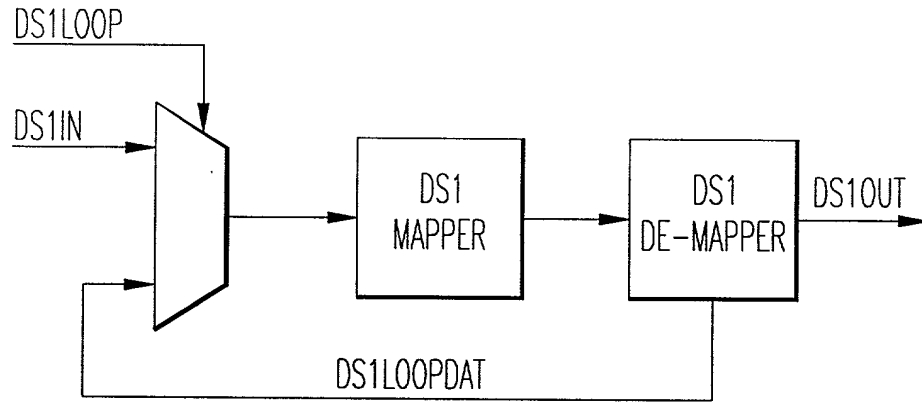


FIG. 45C

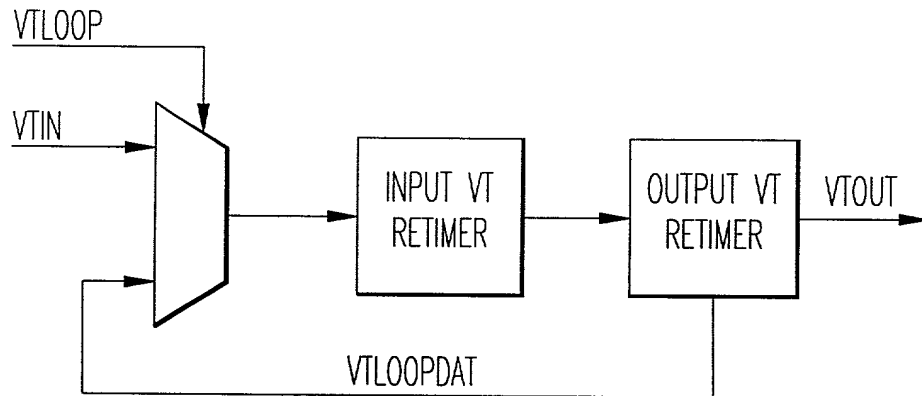


FIG. 45D

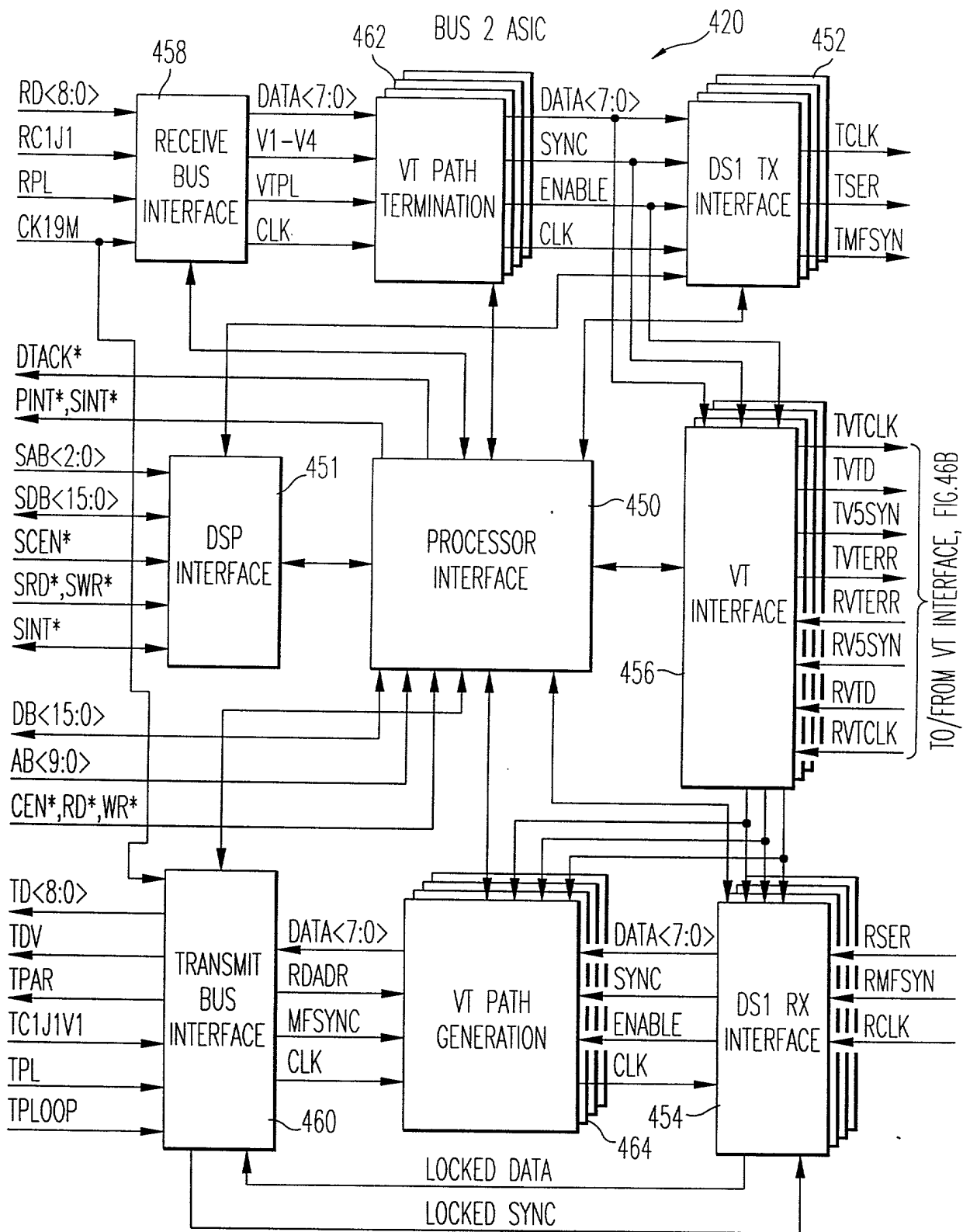


FIG. 46A

FIG. 46B

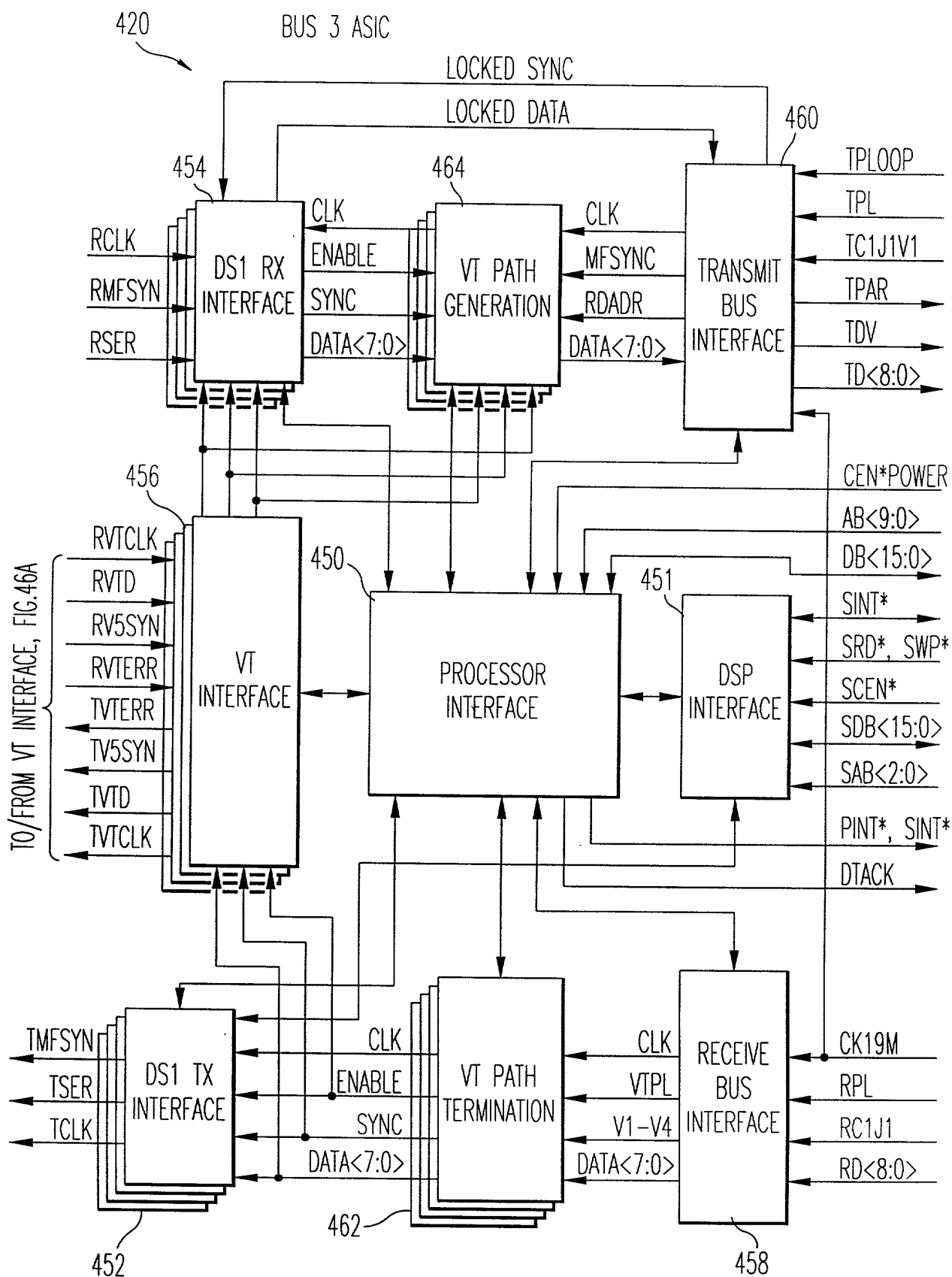


FIG. 46B

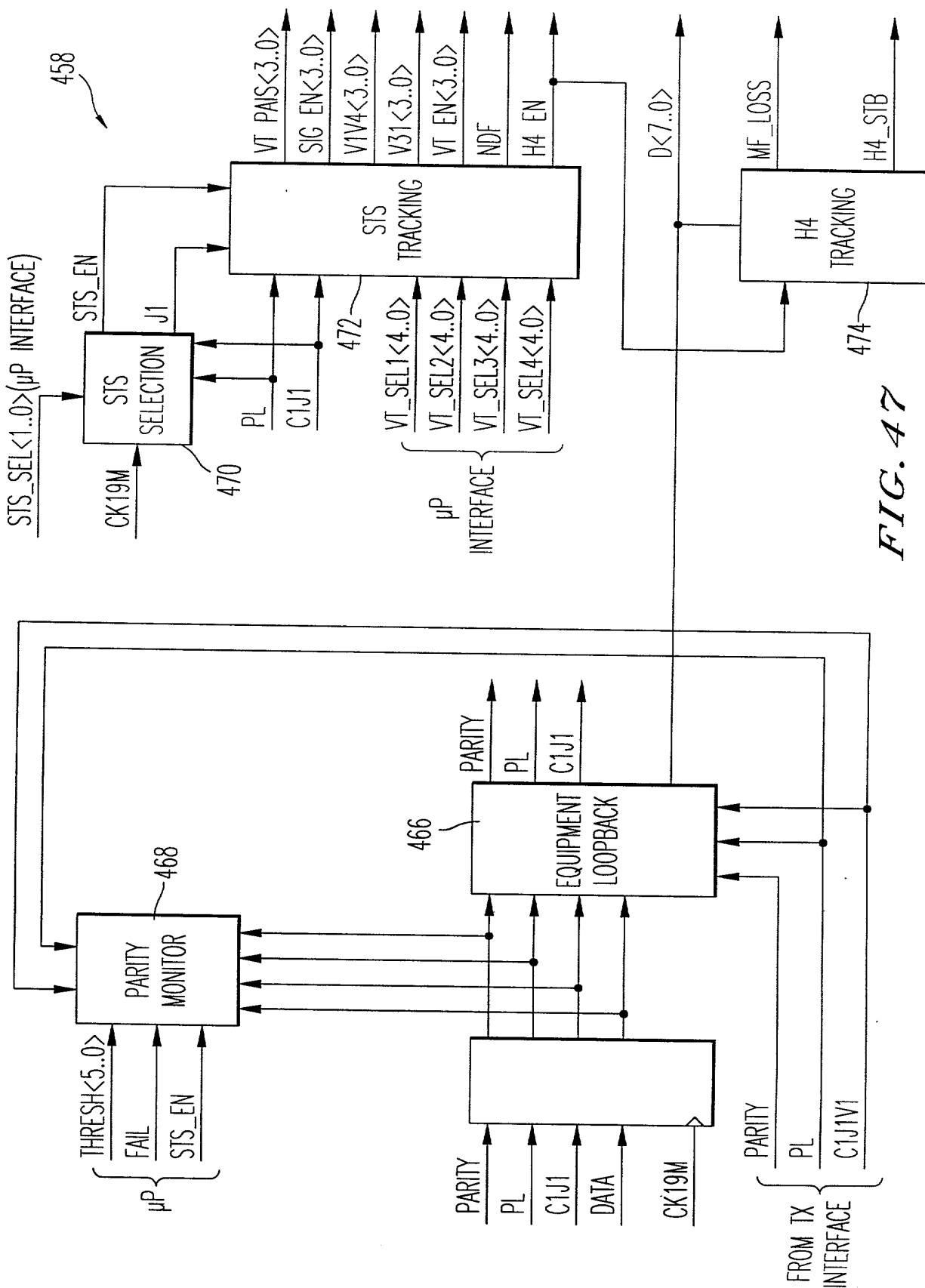


FIG. 47

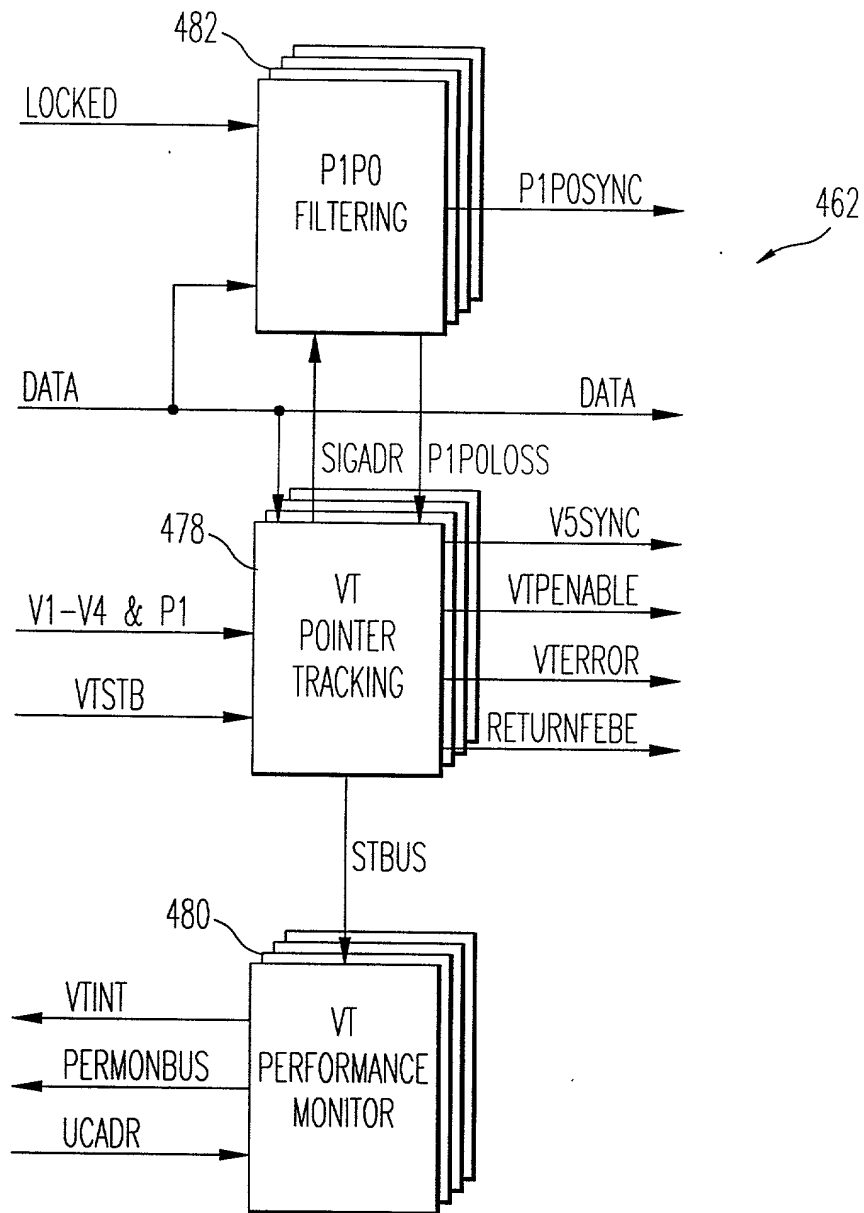
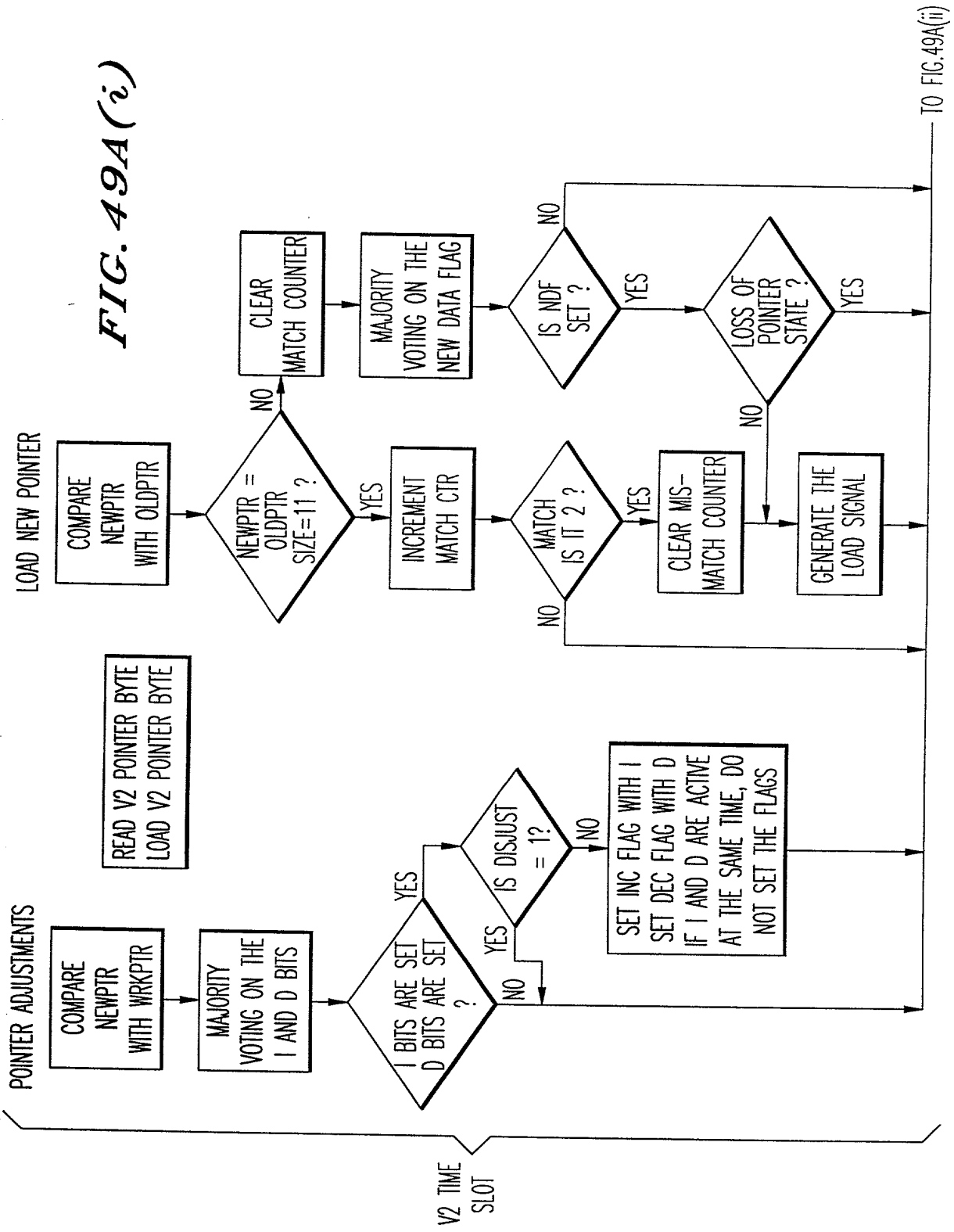
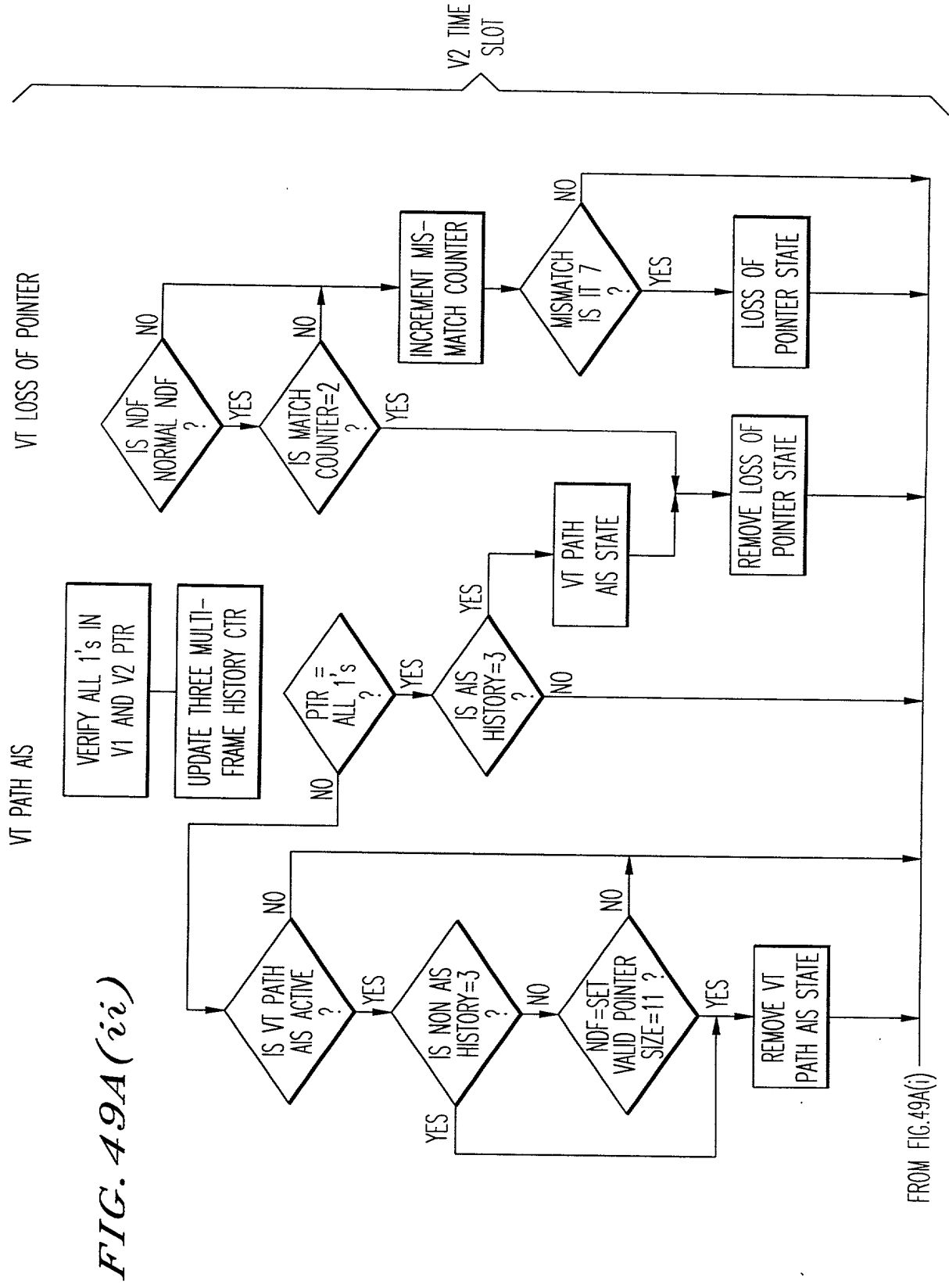


FIG. 48

FIG. 49A(i)
&
FIG. 49A(ii)



TO FIG. 49A(ii)



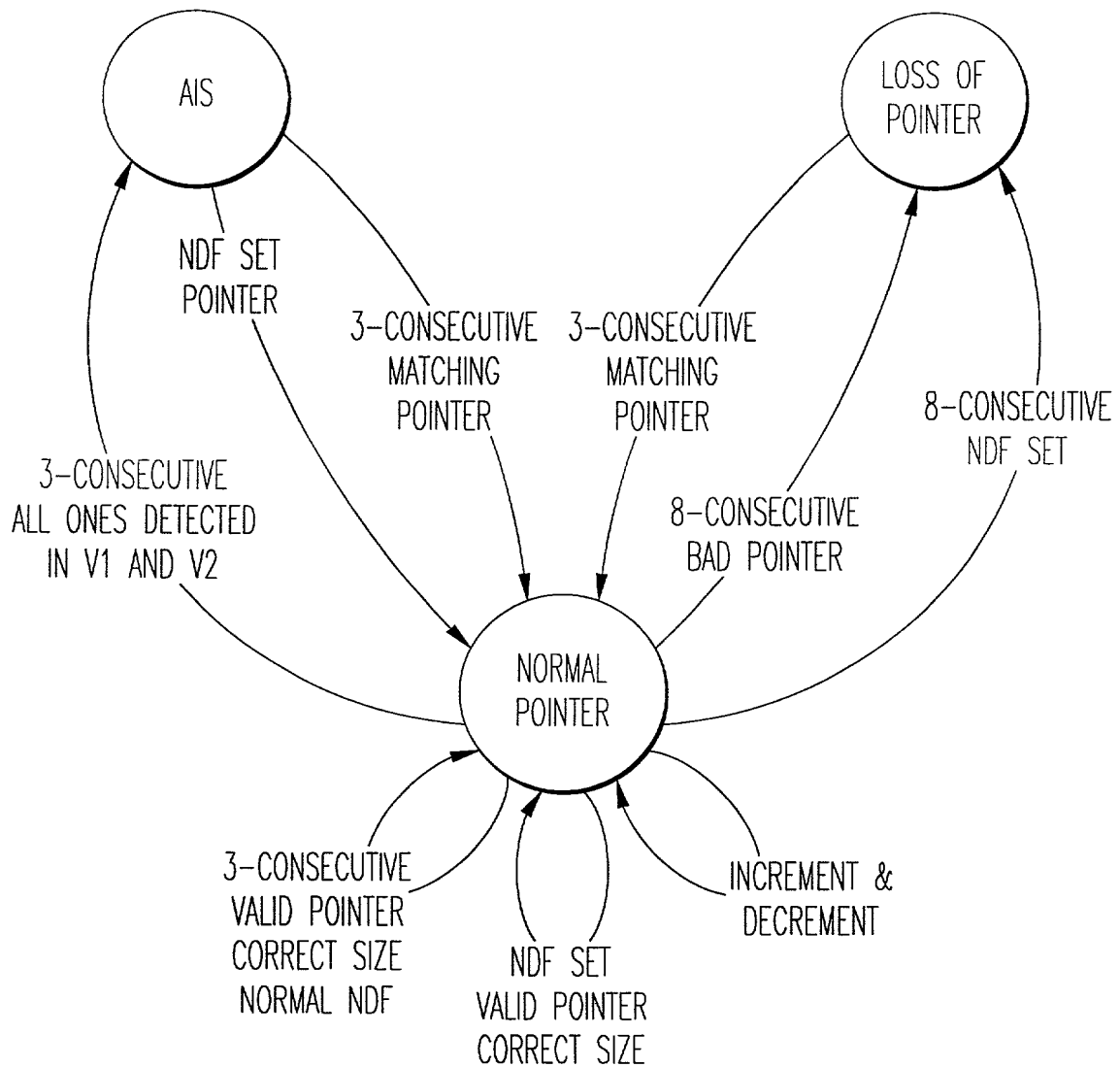
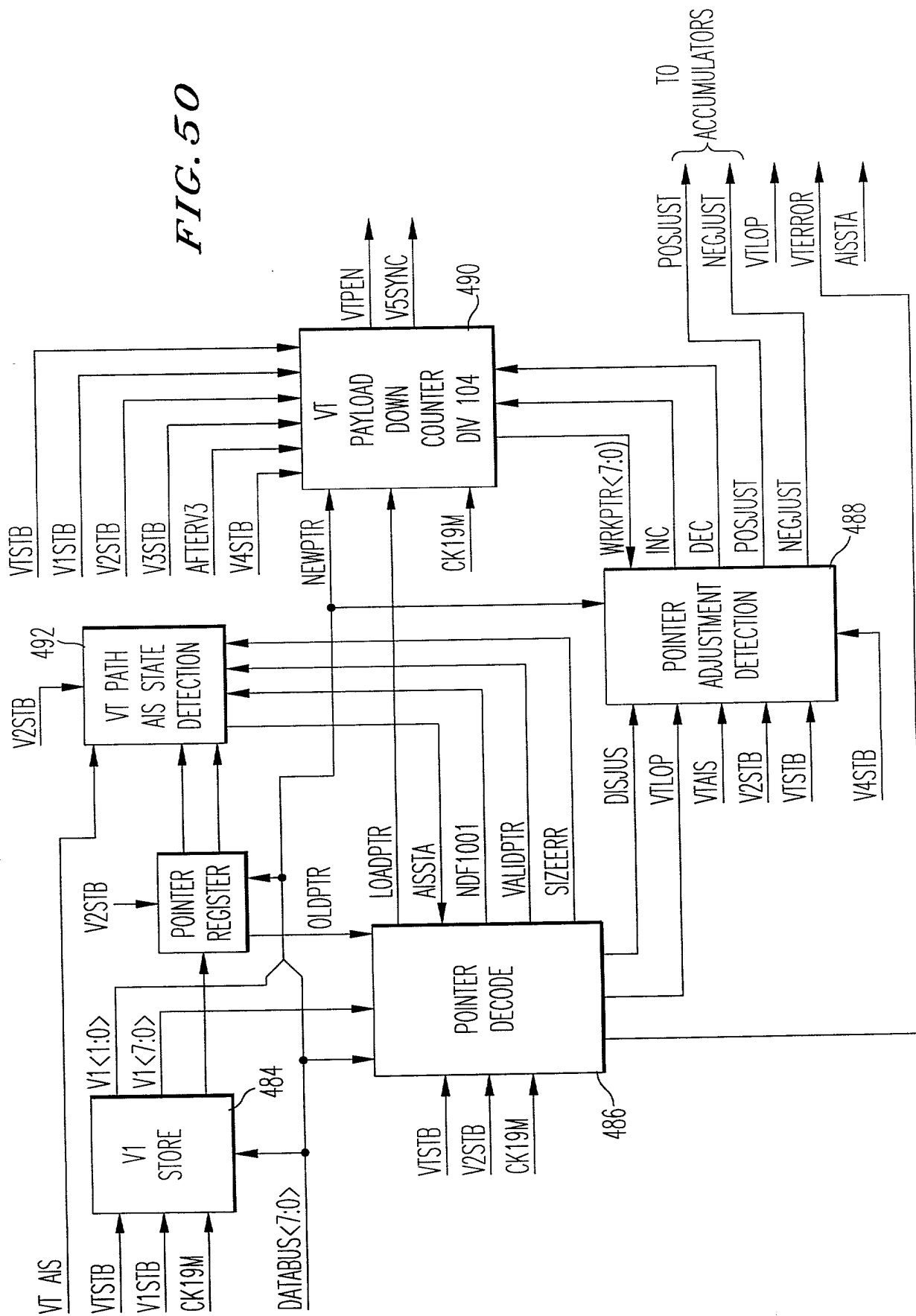


FIG. 49B



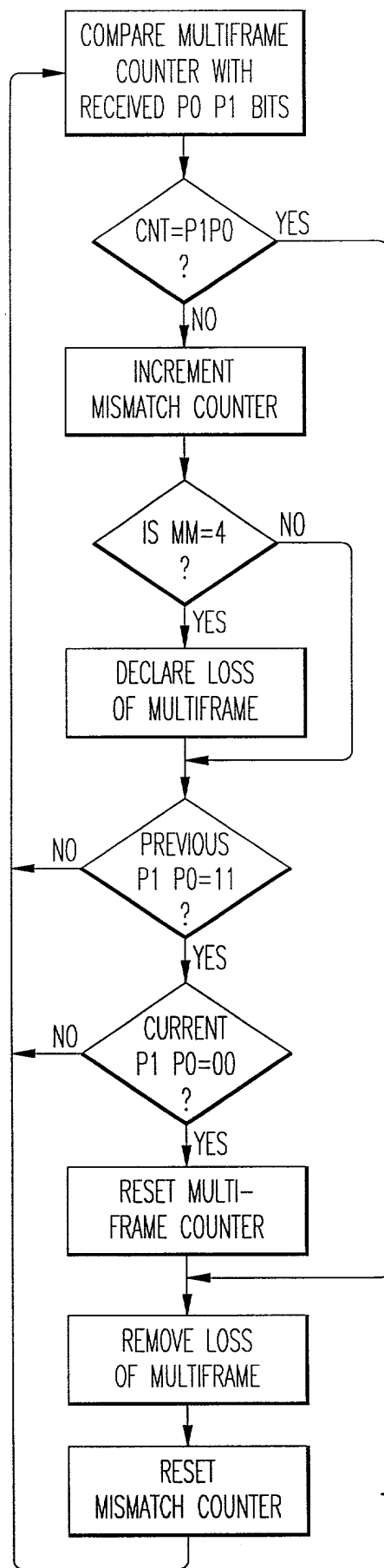
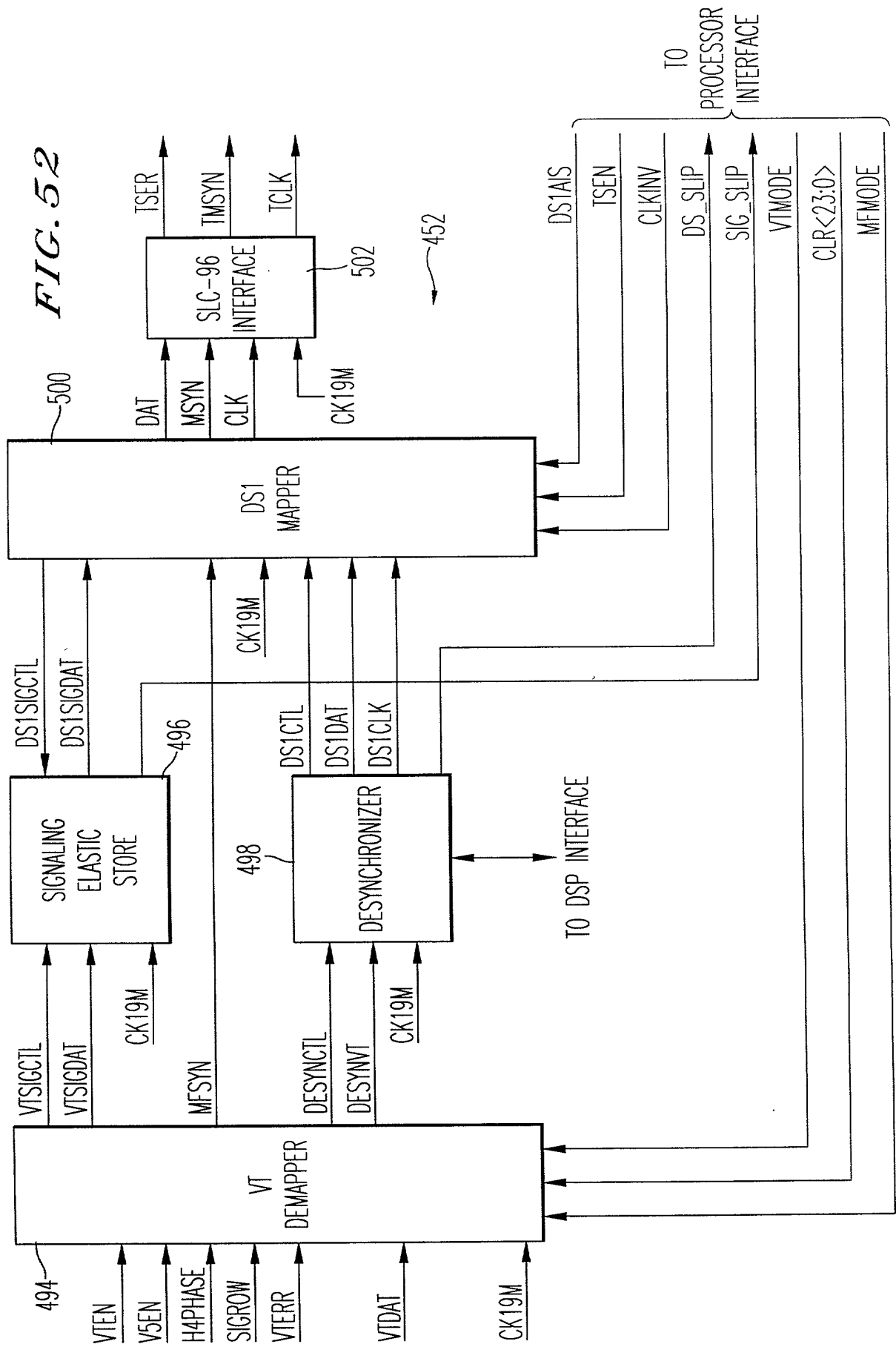


FIG. 51



TO
PROCESSOR
INTERFACE

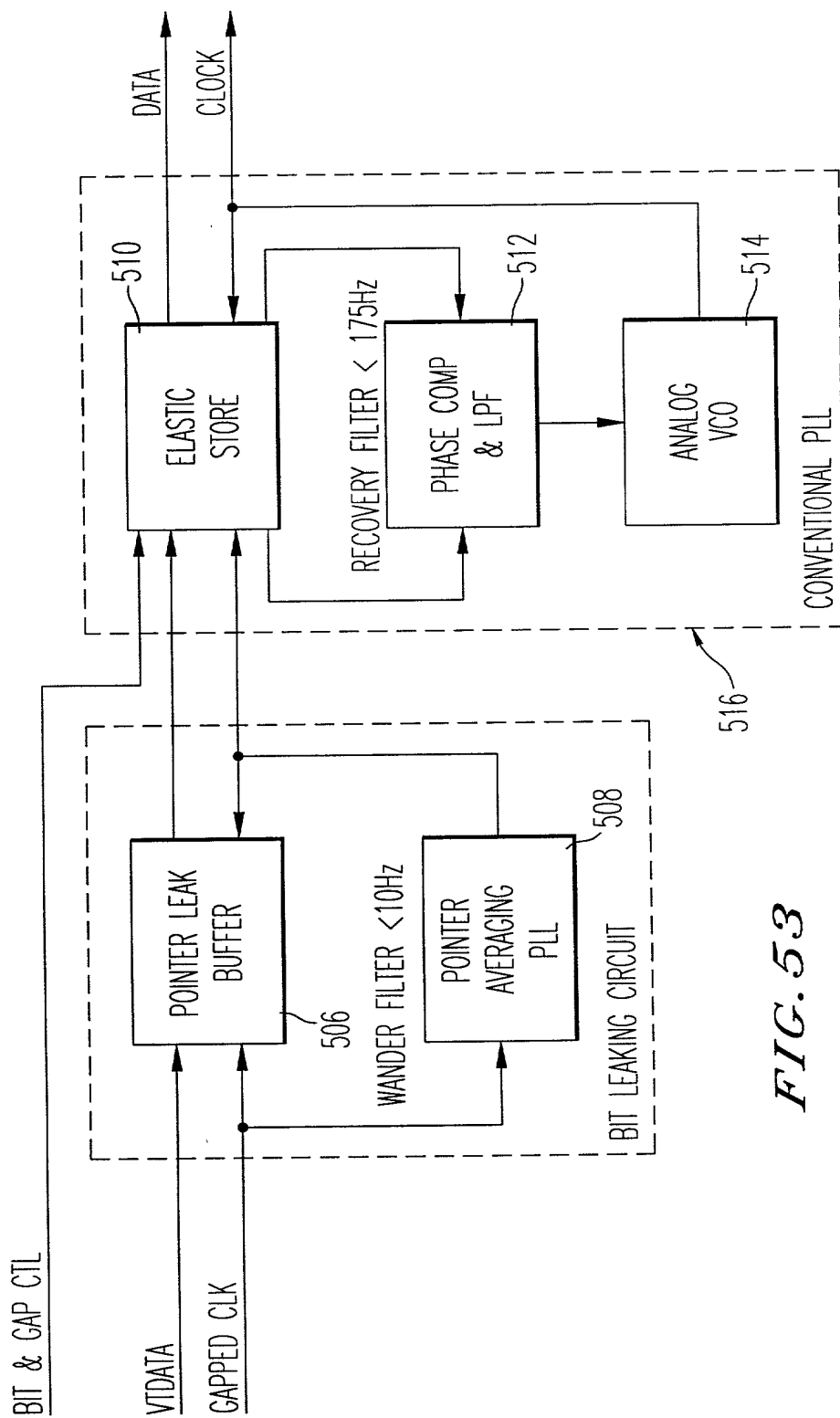
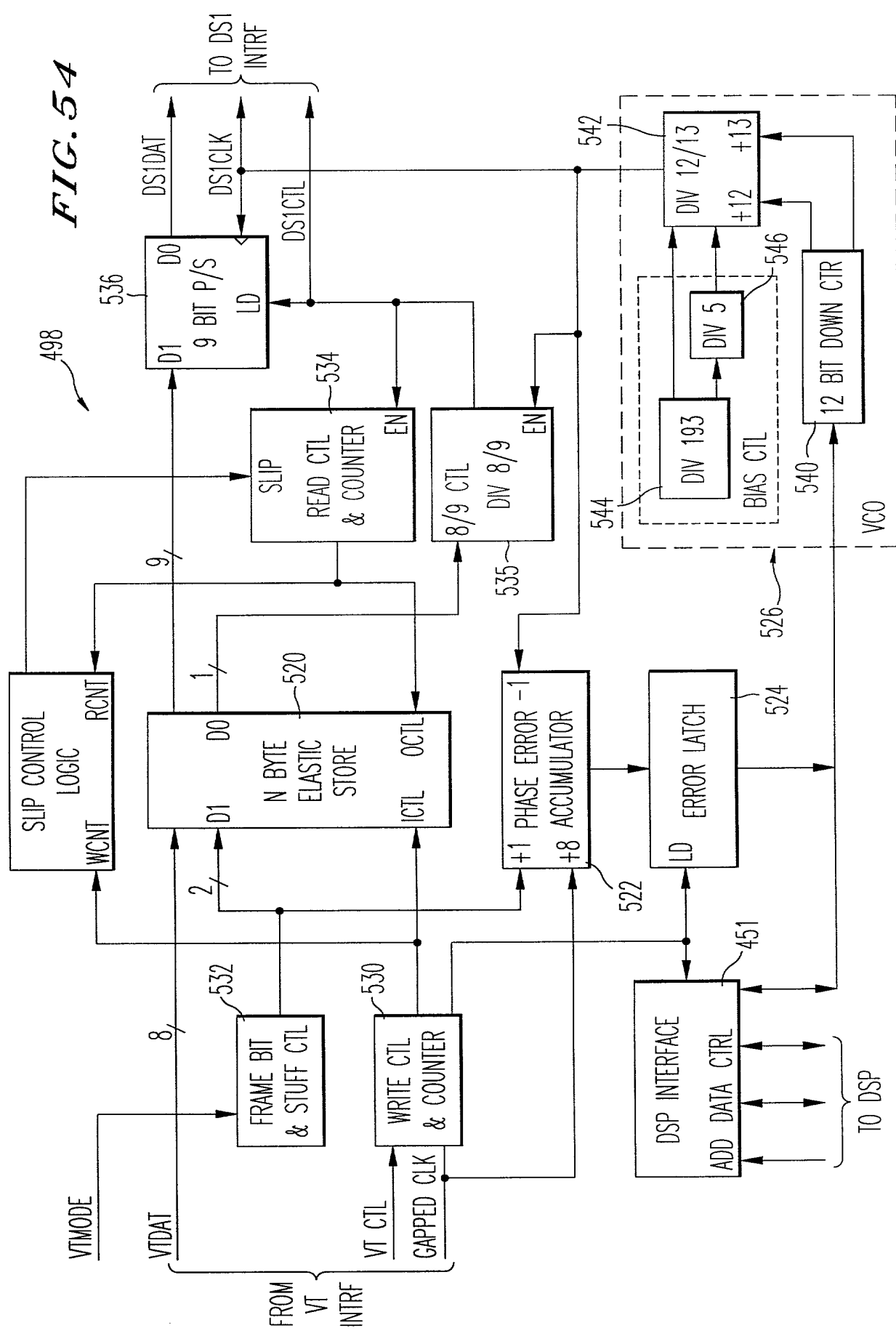


FIG. 53

FIG. 54



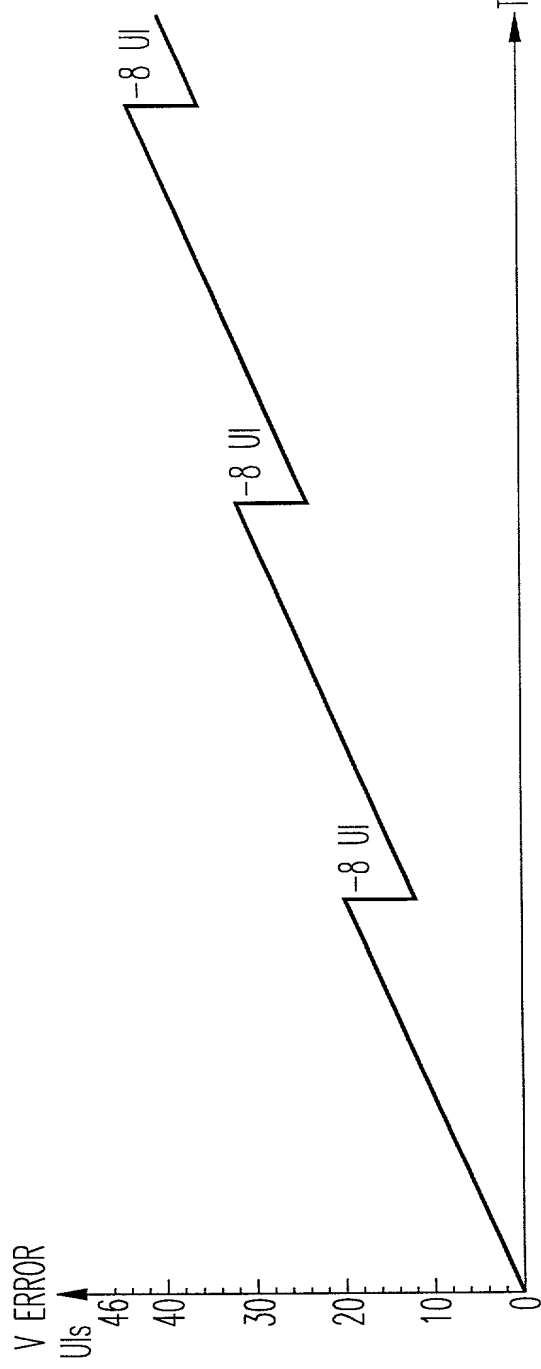


FIG. 55A

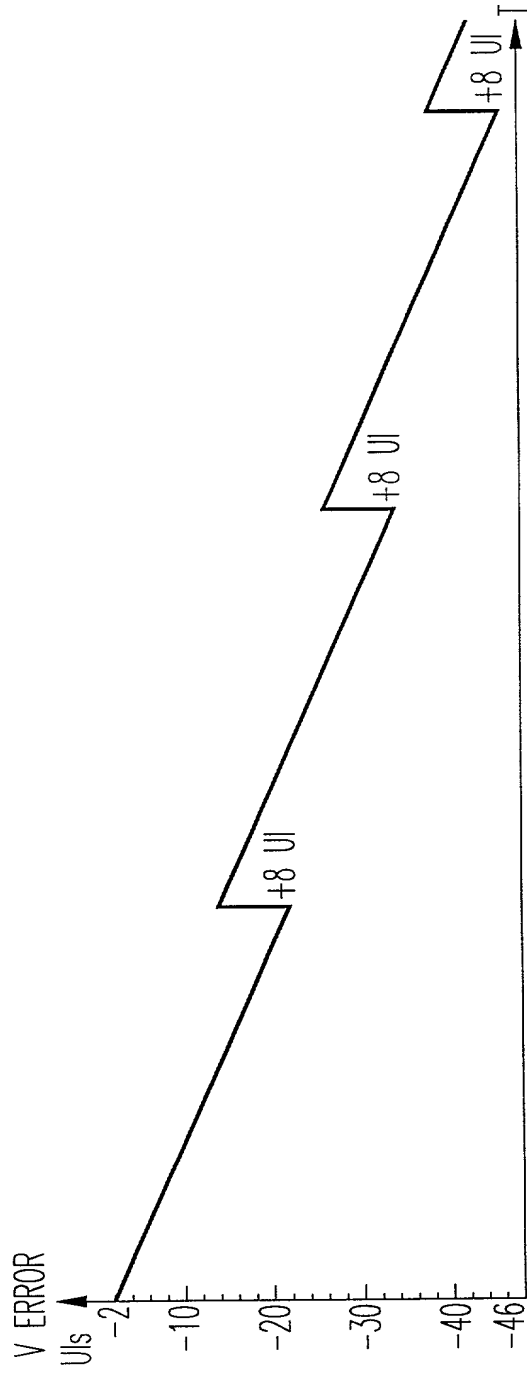


FIG. 55B

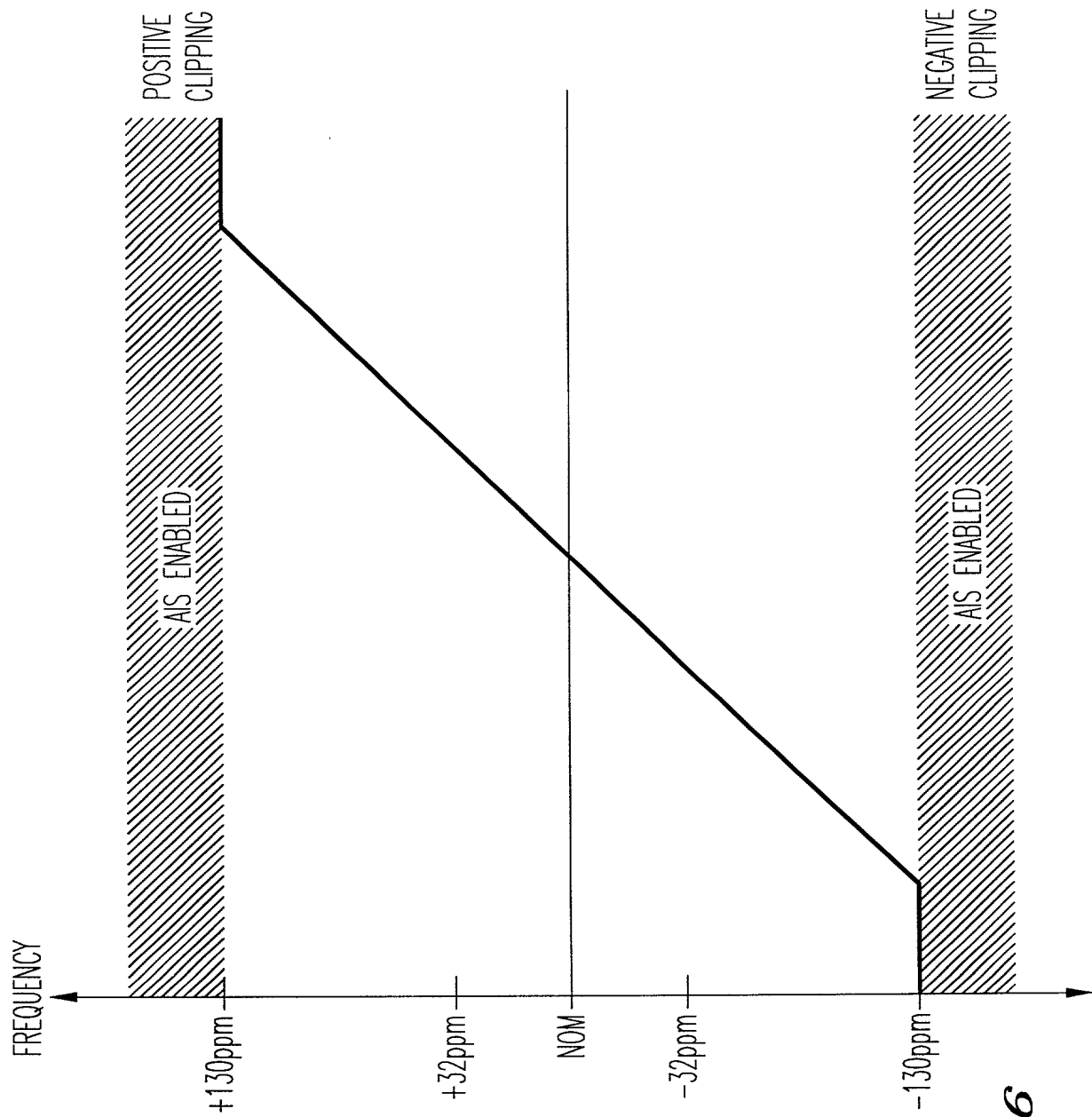


FIG. 56

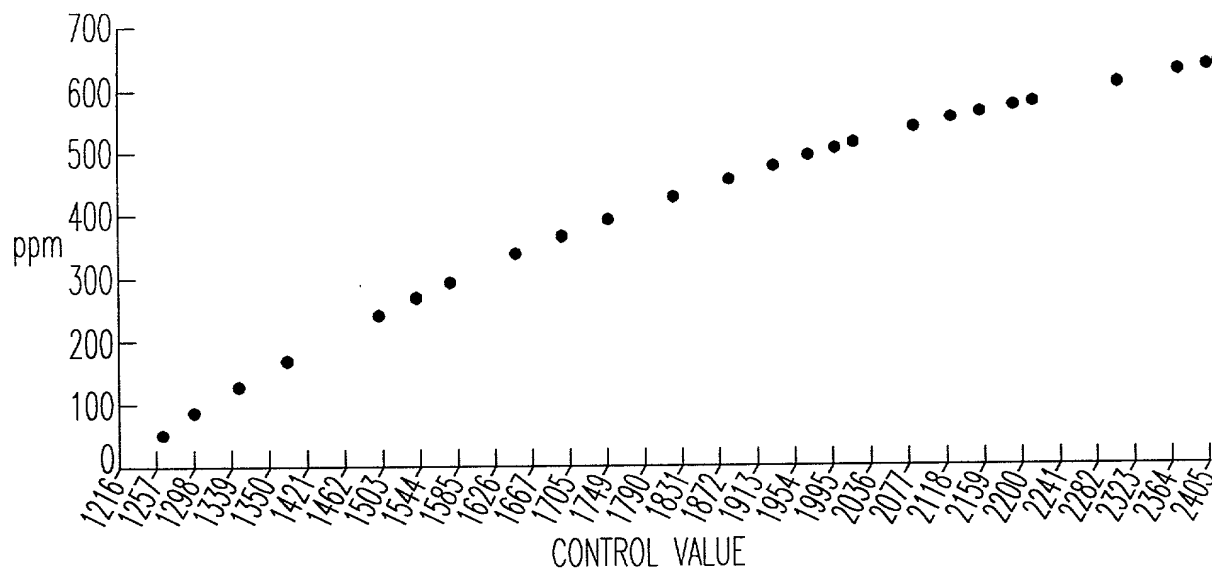


FIG. 57A

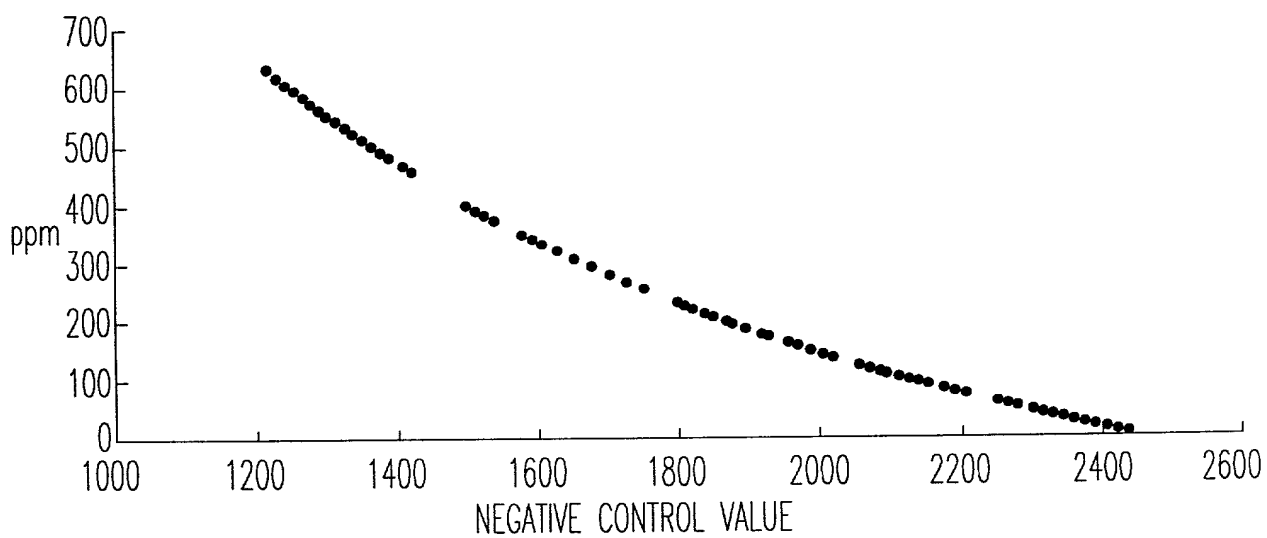


FIG. 57B

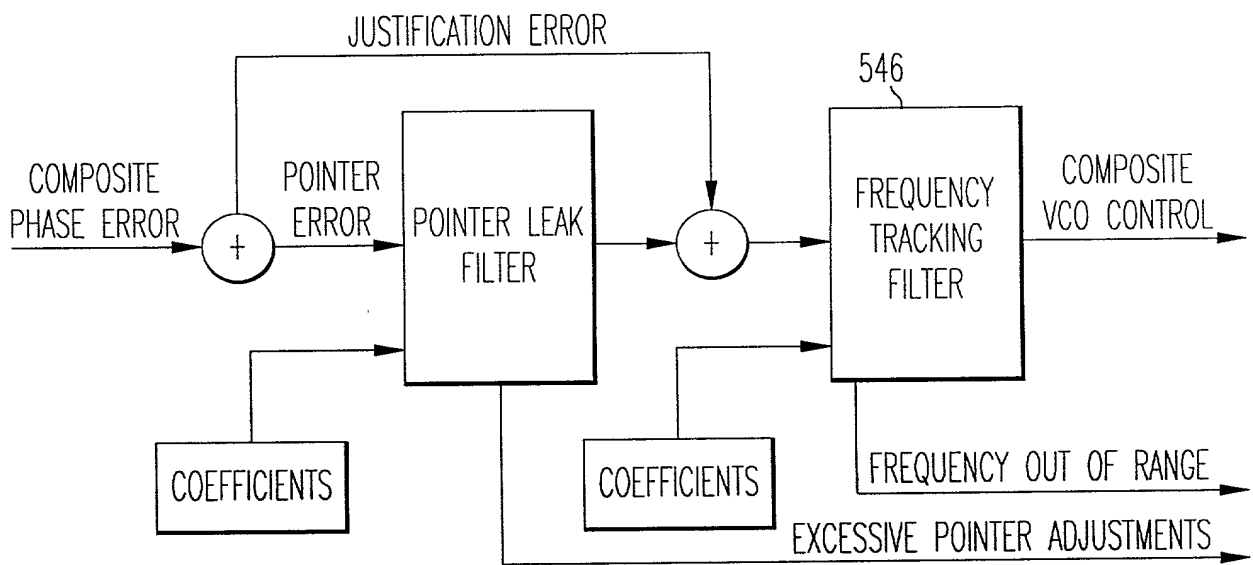


FIG. 58

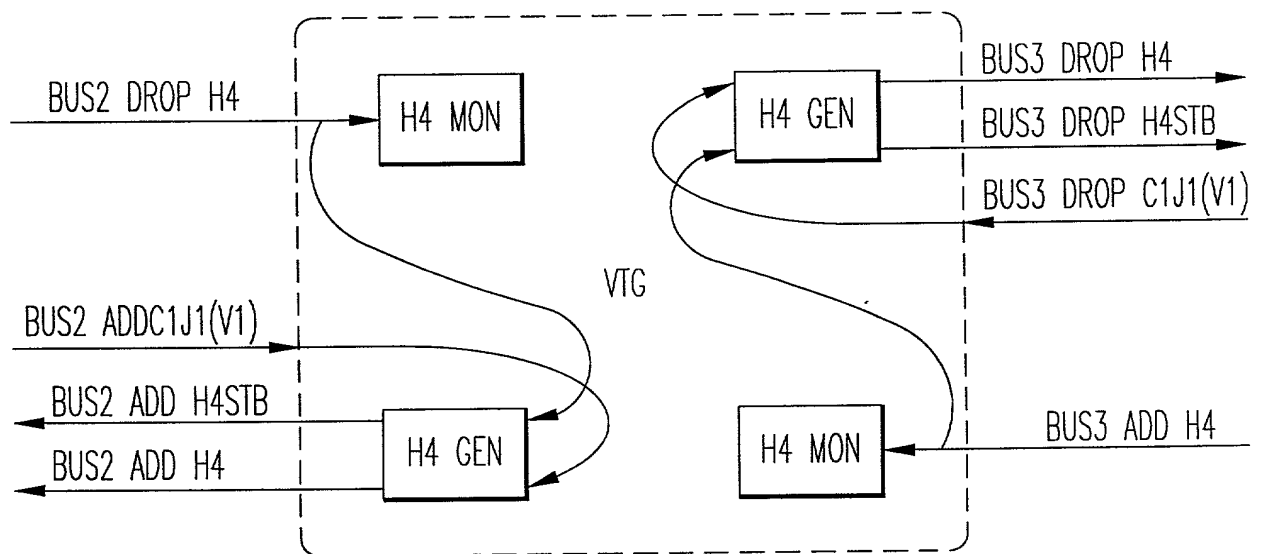


FIG. 61

MULTI-FRAME	FRAME	FS-BIT (SF MODE)	FS-BIT (SLC-96 MODE)
1	2	0	0
1	4	0	0
1	6	1	1
1	8	1	1
1	10	1	1
1	12	0	0
2	2	0	0
2	4	0	0
2	6	1	1
2	8	1	1
2	10	1	1
2	12	0	C1
3	2	0	C2
3	4	0	C3
3	6	1	C4
3	8	1	C5
3	10	1	C6
3	12	0	C7
4	2	0	C8
4	4	0	C9
4	6	1	C10
4	8	1	C11
4	10	1	0
4	12	0	1
5	2	0	0
5	4	0	M1
5	6	1	M2
5	8	1	M3
5	10	1	A1
5	12	0	A2
6	2	0	S1
6	4	0	S2
6	6	1	S3
6	8	1	S4
6	10	1	1
6	12	0	0

FIG. 59

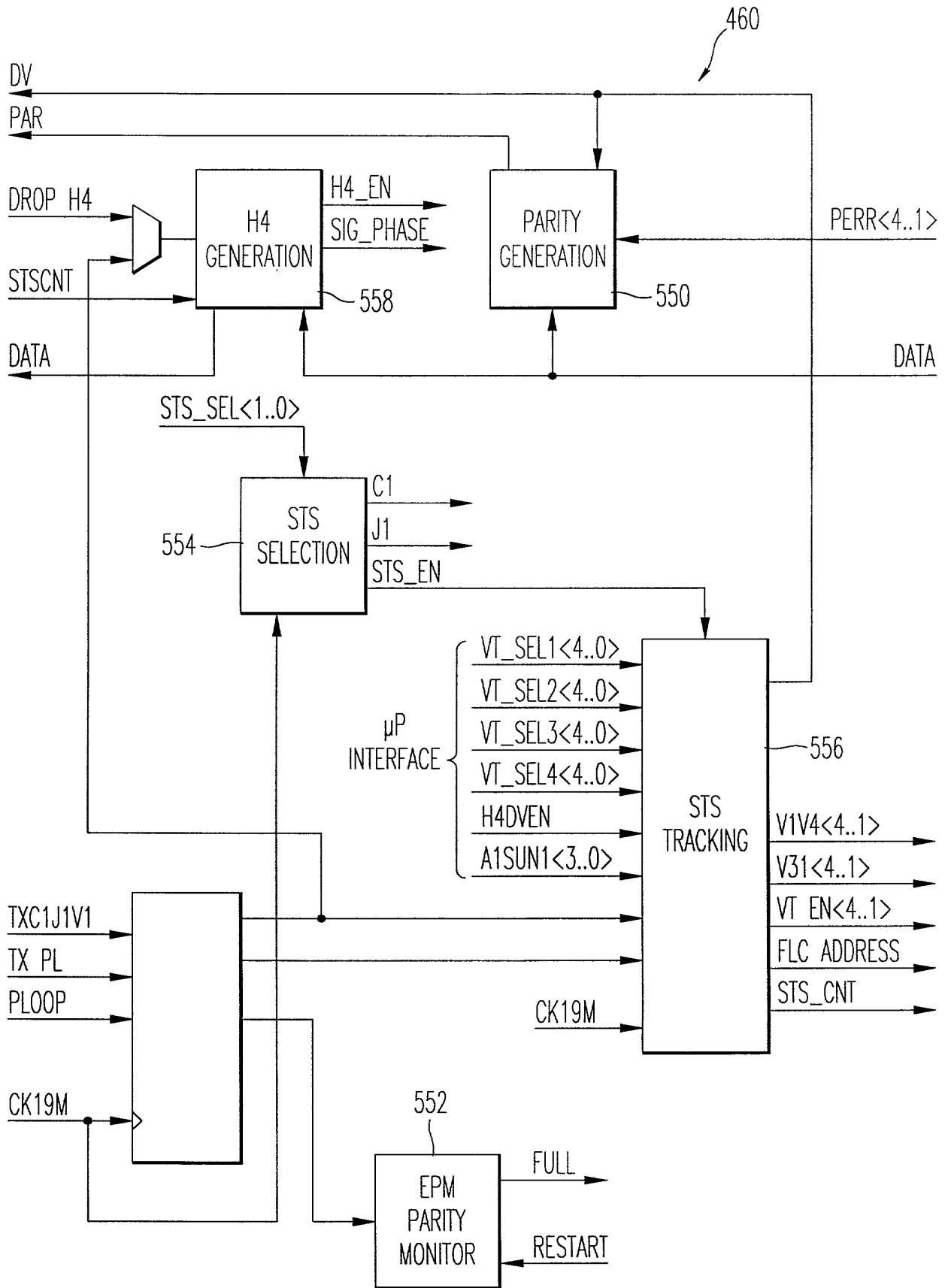


FIG. 60

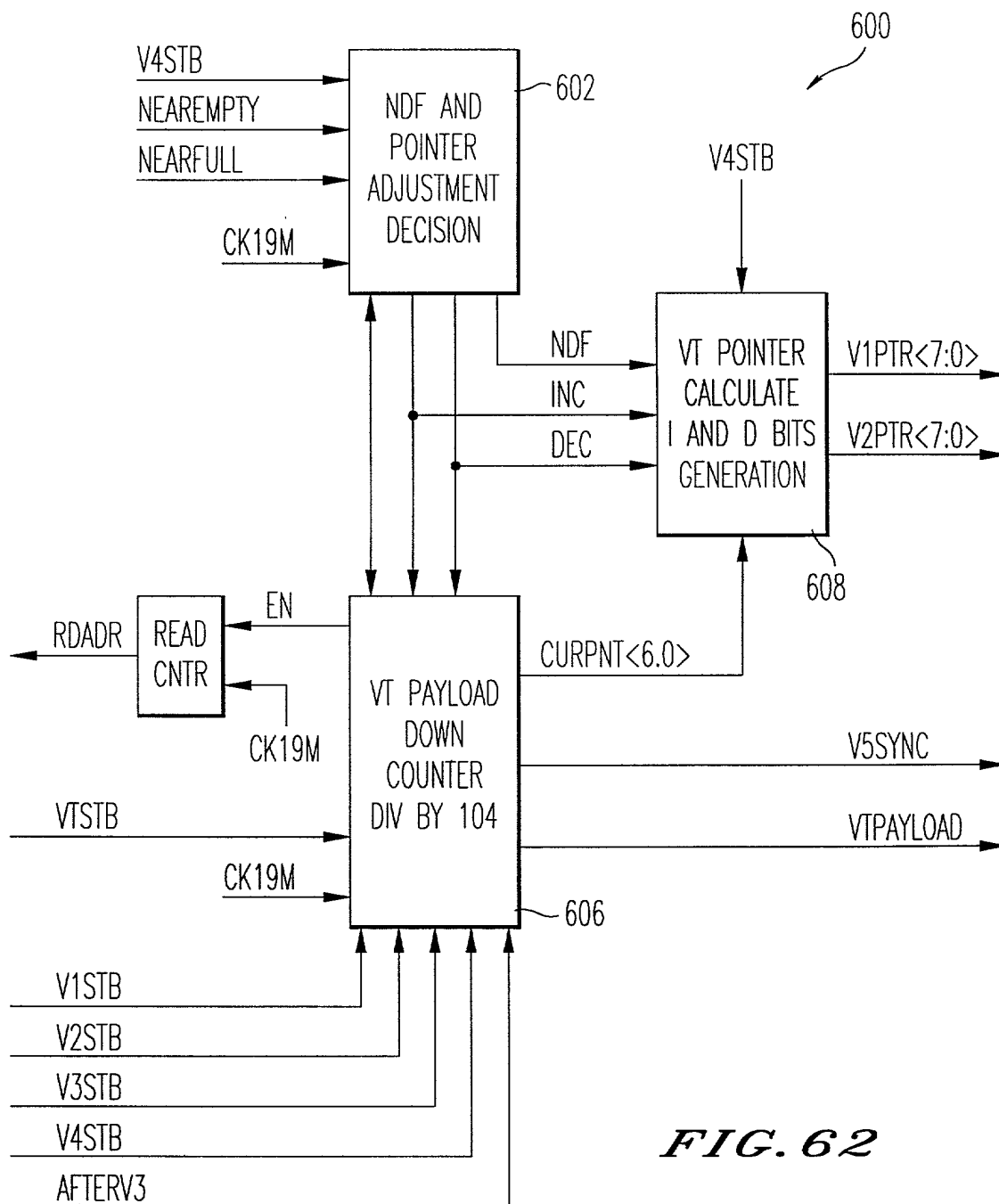
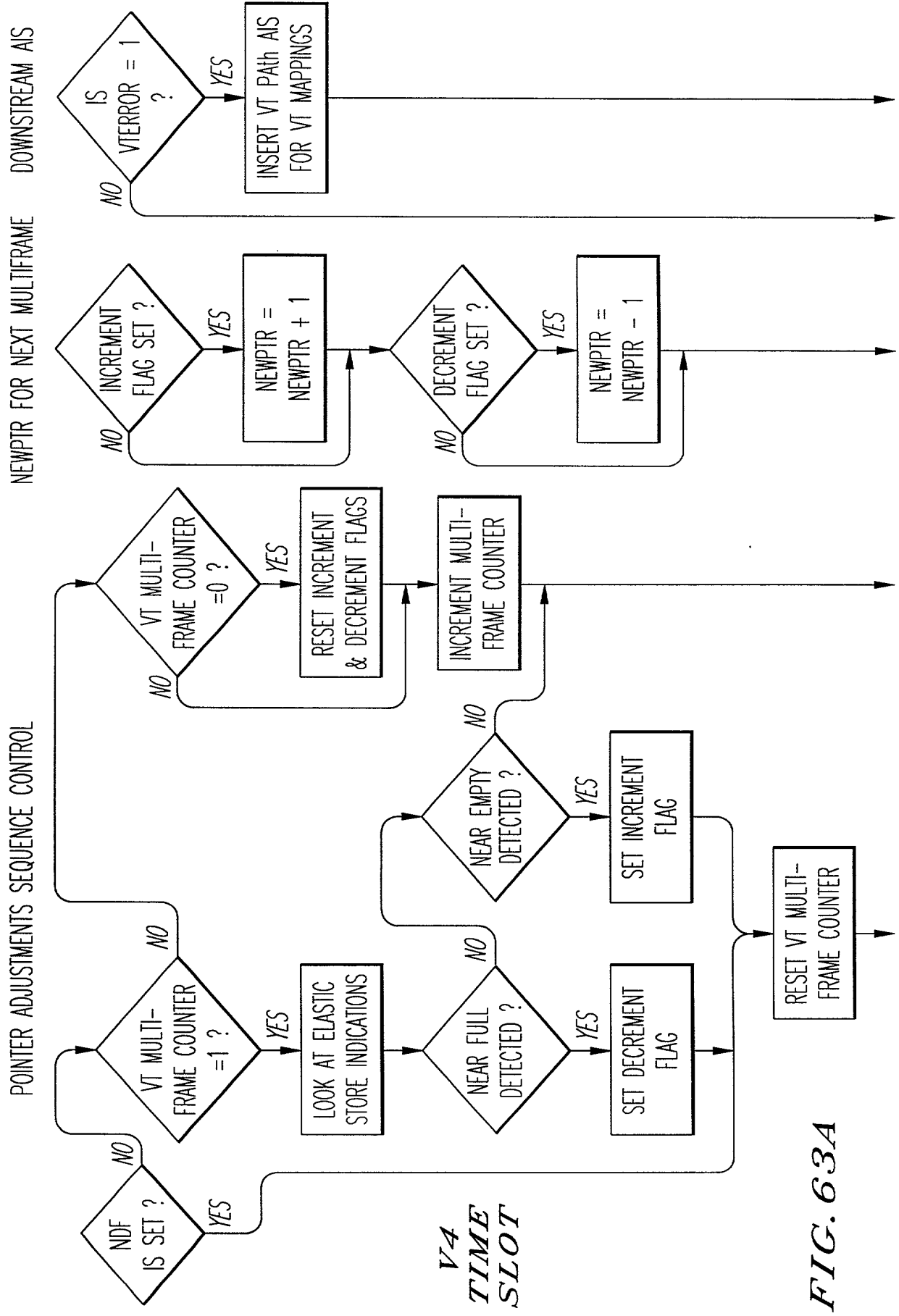
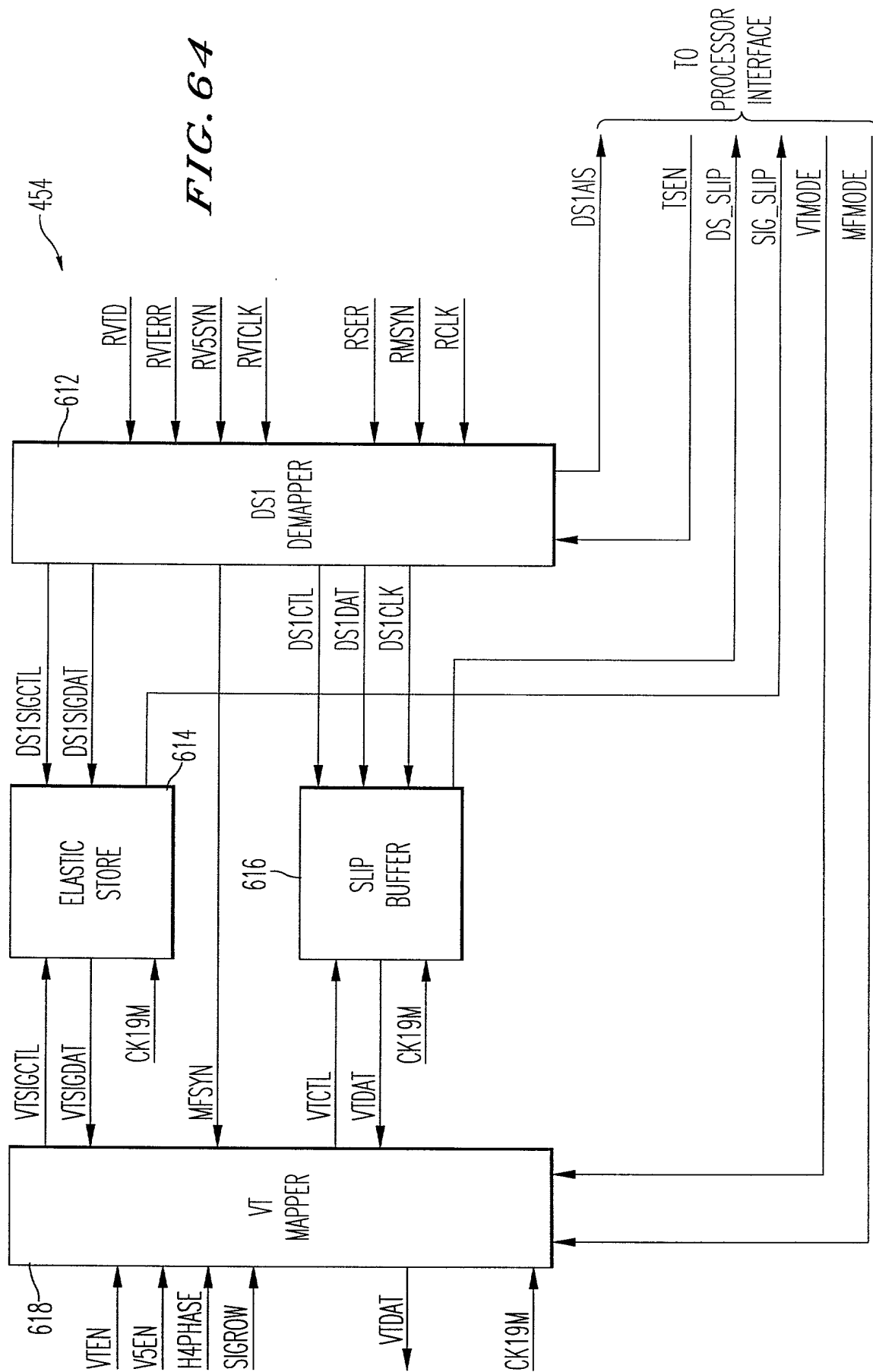


FIG. 62





The diagram illustrates the timing of the 68000 microprocessor's address and bus signals during memory access. It is divided into three sections based on the state of the ARPL and BRPL signals.

- Top Section: NO POINTER ADJUSTMENTS**
 - CK19M:** A periodic clock signal.
 - ARD<8:0>:** Address data bus, showing a sequence of 15 data words (H1 1, H1 2, H1 3, H2 1, H2 2, H2 3, H3 1, H3 2, H3 3, PL 1, PL 2, PL 3, 1, 2, 3, 1).
 - BRD<8:0> (INPUTS):** Bus data bus, showing the same sequence of 15 data words as ARD.
 - ARPL:** Address register pointer, showing a sequence of 15 data words (1, 2, 3, 1, 2, 3, 1, 2, 3, 1, 2, 3, 1, 2, 3, 1).
 - BRPL (INPUT):** Bus register pointer, showing a sequence of 15 data words (1, 2, 3, 1, 2, 3, 1, 2, 3, 1, 2, 3, 1, 2, 3, 1).
- Middle Section: NEGATIVE POINTER ADJUSTMENTS**
 - CK19M:** A periodic clock signal.
 - ARD<8:0>:** Address data bus, showing a sequence of 15 data words (H1 1, H1 2, H1 3, H2 1, H2 2, H2 3, H3 1, H3 2, H3 3, STF 1, PL 2, PL 3, 1, 2, 3, 1).
 - BRD<8:0> (INPUTS):** Bus data bus, showing the same sequence of 15 data words as ARD.
 - ARPL:** Address register pointer, showing a sequence of 15 data words (1, 2, 3, 1, 2, 3, 1, 2, 3, 1, 2, 3, 1, 2, 3, 1).
 - BRPL (INPUT):** Bus register pointer, showing a sequence of 15 data words (1, 2, 3, 1, 2, 3, 1, 2, 3, 1, 2, 3, 1, 2, 3, 1).
- Bottom Section: POSITIVE POINTER ADJUSTMENTS**
 - CK19M:** A periodic clock signal.
 - ARD<8:0>:** Address data bus, showing a sequence of 15 data words (H1 1, H1 2, H1 3, H2 1, H2 2, H2 3, H3 1, H3 2, H3 3, STF 1, PL 2, PL 3, 1, 2, 3, 1).
 - BRD<8:0> (INPUTS):** Bus data bus, showing the same sequence of 15 data words as ARD.
 - ARPL:** Address register pointer, showing a sequence of 15 data words (1, 2, 3, 1, 2, 3, 1, 2, 3, 1, 2, 3, 1, 2, 3, 1).
 - BRPL (INPUT):** Bus register pointer, showing a sequence of 15 data words (1, 2, 3, 1, 2, 3, 1, 2, 3, 1, 2, 3, 1, 2, 3, 1).

FIG. 66

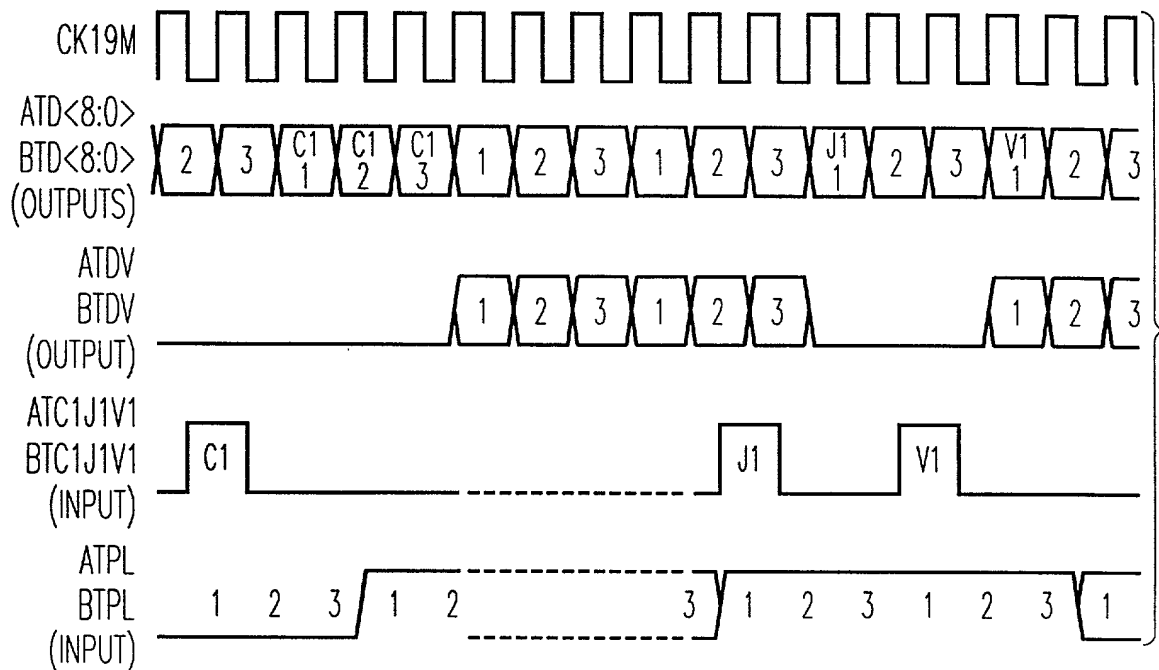


FIG. 67

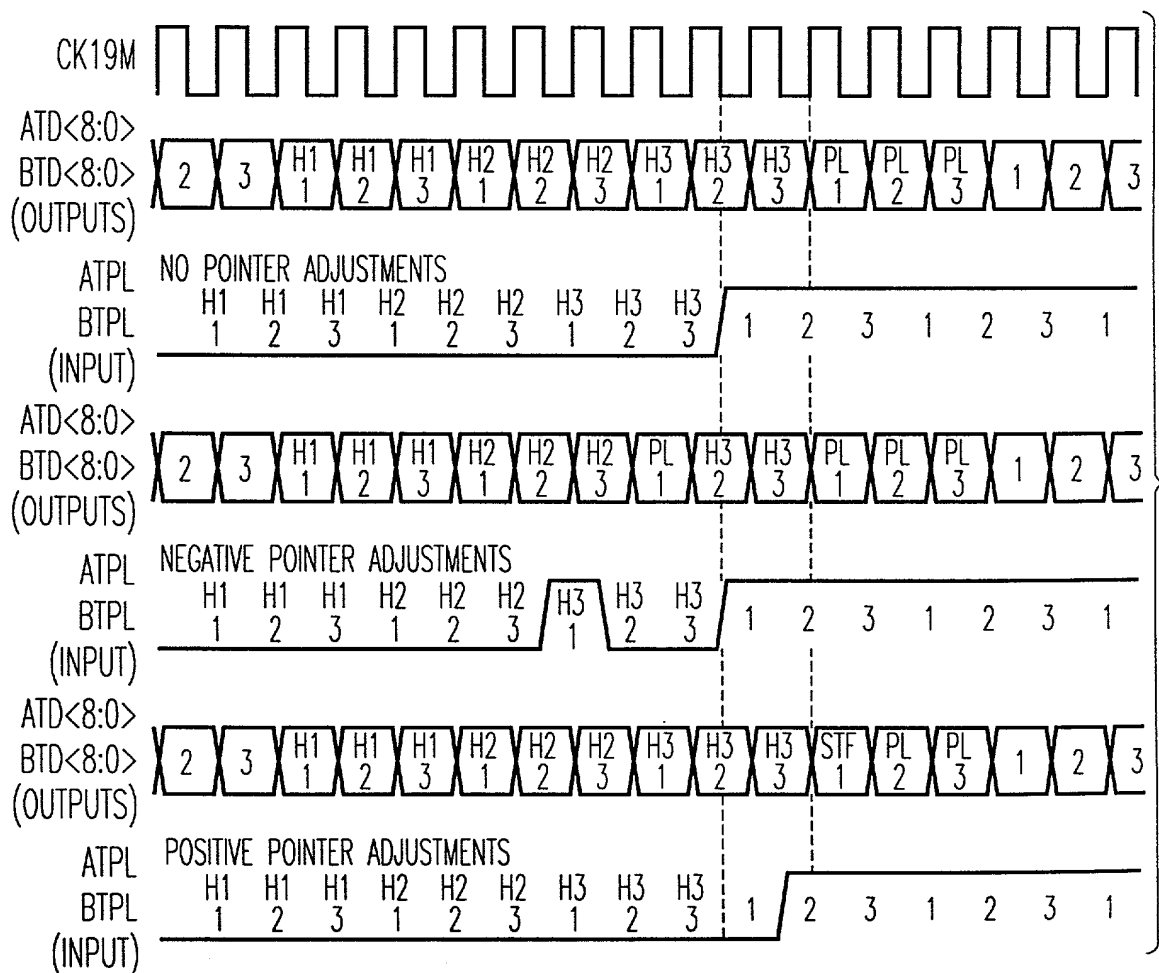


FIG. 68

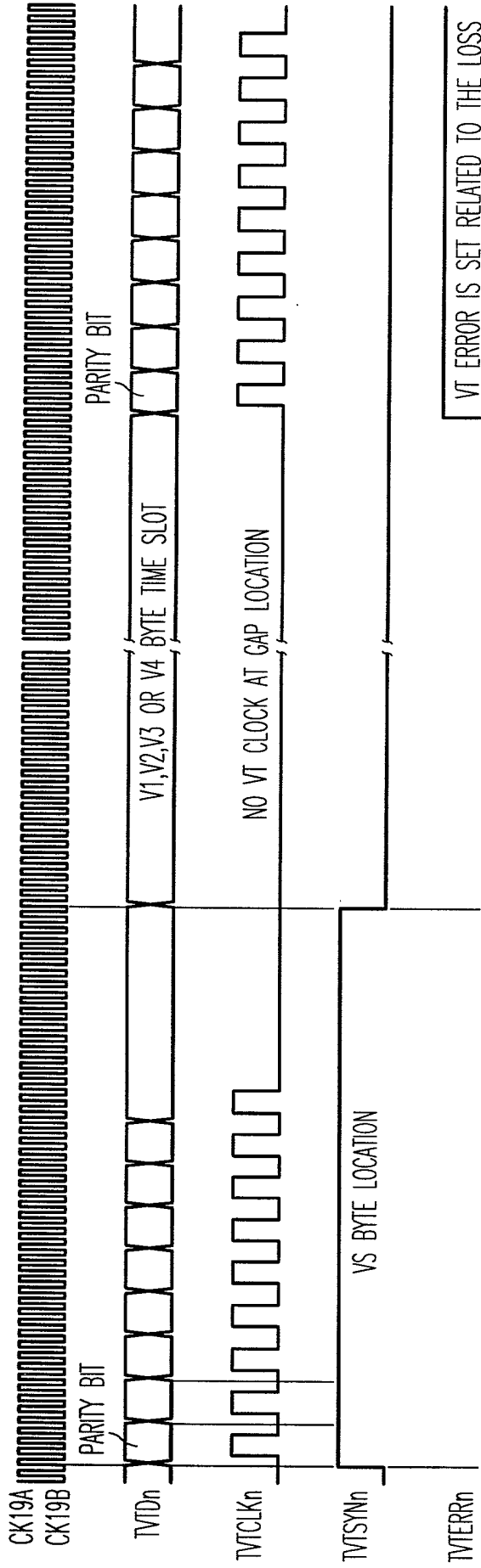


FIG. 69

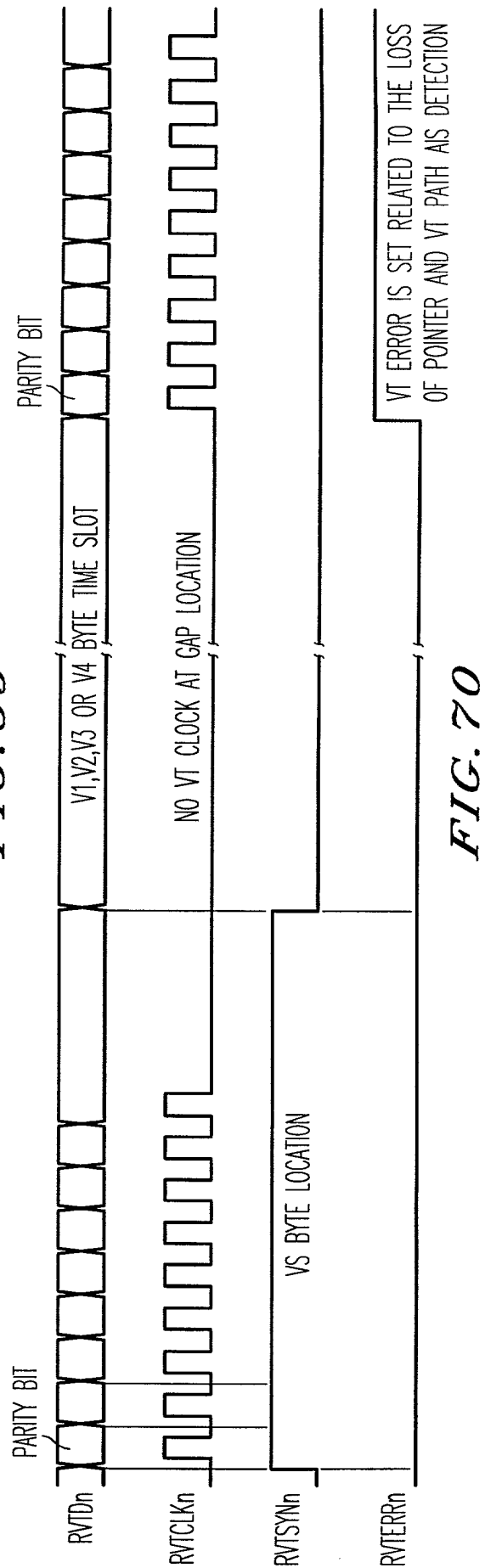


FIG. 70

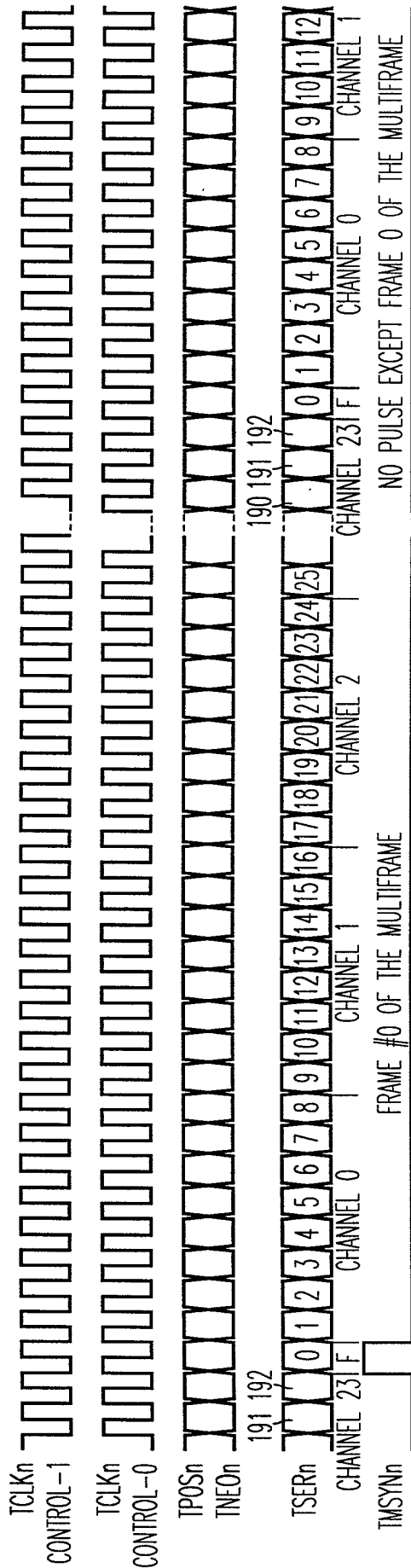


FIG. 71

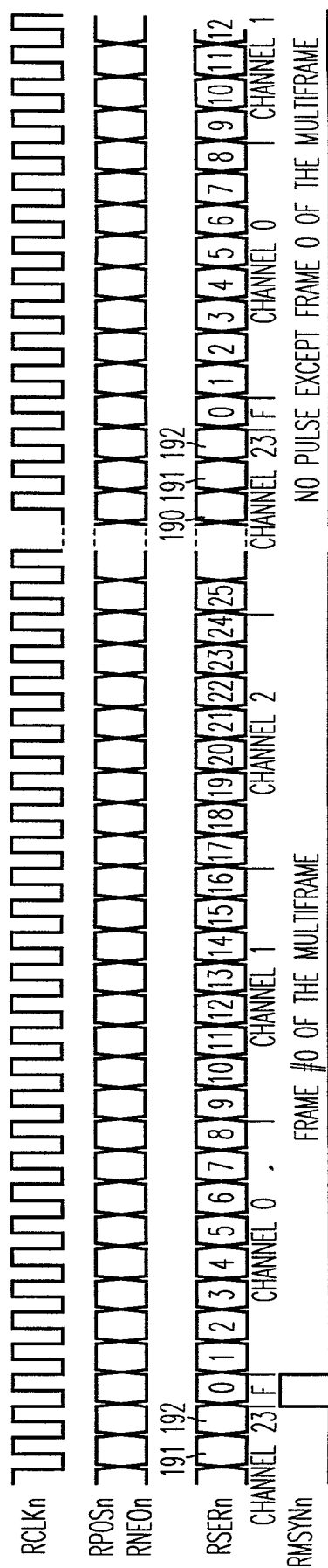


FIG. 72

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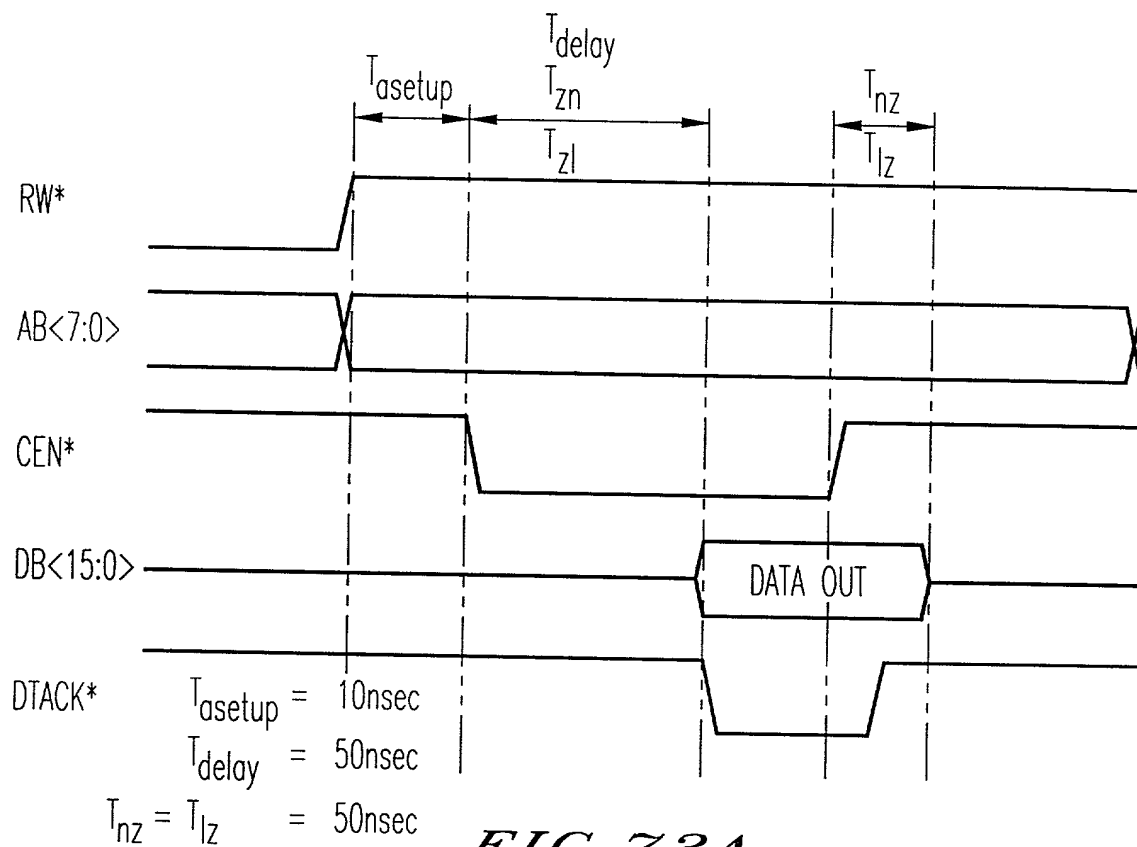


FIG. 73A

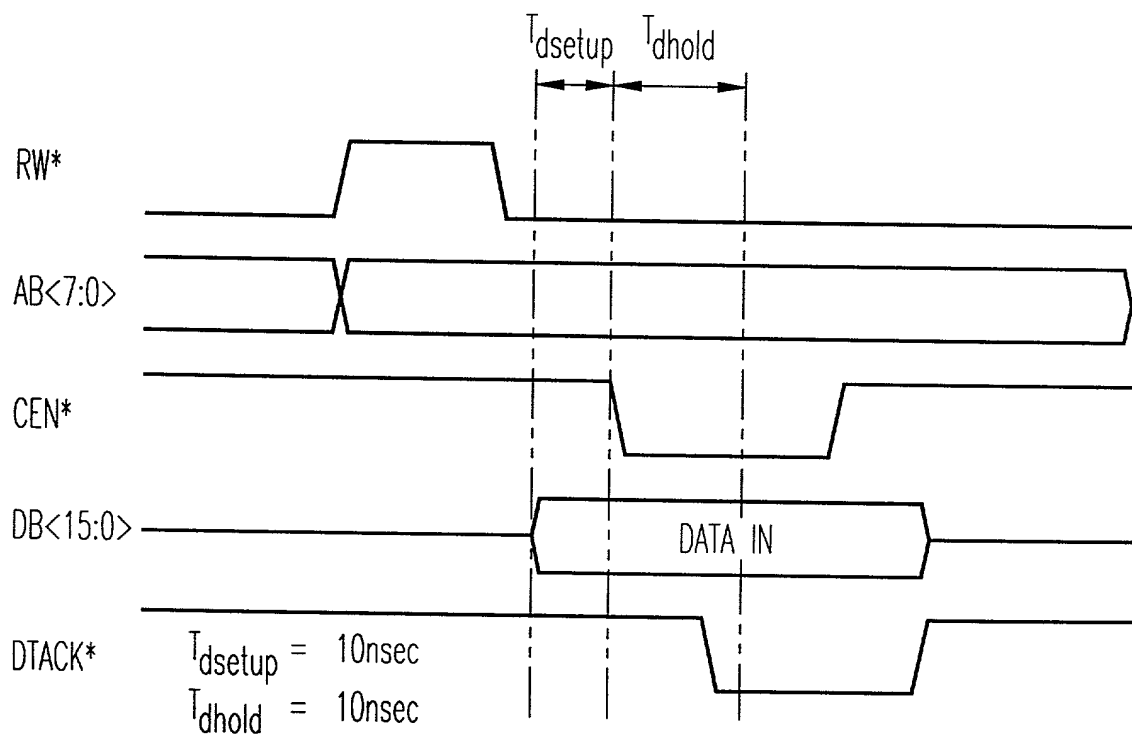


FIG. 73B